In re application of: **Burgener, et al.**

Serial No.: **10/658,154** Group Art Unit: **2816**

Filed: **September 8, 2003** Examiner: **Terry L. Englund**

For: **Low Noise Charge Pump Method and Apparatus**

In accordance with 37 C.F.R. 1.8, I, Barbara S. Kelly, hereby certify that this correspondence and all its attachments are being deposited on **Friday, January 05, 2007** with the U.S. Postal Service with sufficient postage as First Class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Barbara Kelly 1/5/07
Barbara S. Kelly

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDED APPEAL BRIEF

Dear Sirs:

Responsive to the Notification of Non-Compliant Appeal Brief mailed November 2, 2006 in the above-referenced patent application, Appellants hereby submit this Amended Appeal Brief in accordance with 37 CFR 41.37(d). A petition for a two-month extension of time to respond is attached hereto, together with a credit card authorization for the associated fee. This Amended Appeal Brief corrects the deficiencies in the original brief as set forth in the Notification. The Summary of Claimed Subject Matter is hereby amended to include references to the specification page and line number, in addition to the previously included references to figures and paragraph number, for each independent claim involved in the appeal. The Appeal Brief is also hereby amended to include an issue summary section in the argument that consolidates certain examination issues applicable to a multiplicity of claims. Other minor amendments are included herein to address typographical errors and improve readability.

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DOCKET NO.: PER-005-PAP

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Burgener, et al.**

Serial No.: **10/658,154** Group Art Unit: **2816**

Filed: **September 8, 2003** Examiner: **Terry L. Englund**
Confirmation No.: **5658**

For: **Low Noise Charge Pump Method and Apparatus**

In accordance with 37 C.F.R. 1.8, I, Barbara S. Kelly, hereby certify that this correspondence and all its attachments are being deposited on Friday, January 05, 2007 with the U.S. Postal Service with sufficient postage as First Class mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Barbara Kelly 1/5/07
Barbara S. Kelly

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDED APPEAL BRIEF TRANSMITTAL LETTER

Transmitted herewith is an Amended Appeal Brief (**161 pages, plus cover and contents, totaling 165 pages**) in reply to the Notification of Non-Compliant Appeal Brief received from the Examiner dated November 2, 2006 for the above-identified application. This Amended Appeal Brief and attached papers constitute a complete and timely brief.

(XX) A Petition for Extension of Time Under 37 CFR 1.136(a)(1), 1 page.

(XX) A USPTO Credit Card Payment Form, authorizing **$225** two-month extension of time ($225 in accordance with 37 CFR 1.136(a)(1)).

(XX) Photocopies of thirty-two (32) references.

(XX) The Commissioner is hereby authorized to charge any additional filing fees required under 37 CFR 1.16, and any additional patent application processing fees under 37 CFR 1.17 or under 37 CFR 1.20(d), and to construe this paper as including a petition to extend by the number of months necessary to make this paper timely filed.

(XX) Please charge any deficiency or credit any overpayment to Deposit Account No **50-0490**.

Date: 1/5/2007
January 5, 2007

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I. REAL PARTY IN INTEREST

The real party in interest is PEREGRINE SEMICONDUCTOR CORPORATION, the assignee of record, a Delaware corporation based in San Diego, CA.

II. RELATED APPEALS AND INTERFERENCES

On information and belief, there are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-67 are pending. Claim 11 stands allowed, and Claim 26 stands allowable but objected to. Claims 1-10, 12-25, and 27-67 stand rejected.

Appeal is taken of all rejections of Claims 1-10, 12-25, and 27-67.

IV. STATUS OF AMENDMENTS

An Amendment After Final Rejection was mailed on October 11, 2005. Entry was refused. As such, the claims presently pending for purposes of this Appeal are those submitted in the Appellants' first Amendment, which was mailed April 1, 2005.

The Appellants' Amendment After Final Rejection proposed amendments to Claims 7, 13-15, 43, 46-48, 51-52, 60, 62 and 64 pursuant to 37 CFR § 1.116(b), on the grounds that these amendments placed the application into condition for allowance, or, alternatively, into better condition for appeal.

Entry of the Amendment After Final Rejection mailed October 11, 2005 is respectfully requested to place the application into condition for allowance. It is respectfully submitted that no proposed amendment adds any further issue requiring consideration, and that each amendment either obviates a rejection by the Examiner under 35 USC § 112, second paragraph, as lacking clarity, or obviates an objection enunciated by the Examiner, thereby reducing the number of issues to be resolved. It is respectfully submitted that none of the proposed amendments adds new matter, or significantly affects the scope of any claim.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is a charge pump circuit, or a corresponding method, having one or more features suitable to reduce excess electrical noise generated by conventional charge pump circuits.

Charge pumps are widely used to generate additional voltages in electronic circuits. However, conventional charge pumps generate electrical "noise." An integrated antenna switch developed by the Appellants needed an additional voltage to bias the active switch devices, but the noise generated by the first (conventional) charge pumps caused the resulting switches to fail regulatory emissions requirements. Accordingly, it became imperative for the Appellants to develop a charge pump that produced far less electrical noise than prior art charge pump designs.

Prior art charge pumps have found high-speed, precisely timed, plural-phase non-overlapping clocks and fast switching elements important for desirable operation, but these standard design features exacerbated the above-described noise problem. The Appellants therefore contravened conventional charge pump design, arriving at the claimed subject matter described below.

V.A Charge Pump Driven by a Three-Stage Current-Starved Ring Oscillator

Apparatus Claim 1 and method Claim 43 each define a charge pump driven by a current-starved ring oscillator clock that has fewer inverter stages than has previously been thought suitable.

V.A.1 Claim 1

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 3-12, and examples: +/- outputs in Fig. 2 at 216/218 and/or 224/226, Fig. 3 at 316/318, Fig. 4 at 404/634, and Fig. 7 at 404/710; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9 as described from page 16 line 27 to page 18 line 3; and 1014/1016 in Fig. 10) **within a circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12 and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) **a plurality of transfer capacitor coupling switches** ("TCCSs," see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, page 15 lines 17-27, and

examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, diode-connected FETs 704 and 706 in Fig. 7, switches 800 and 830 in Figs. 9 and 10), **each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output** (see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Figs. 6 and 7, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10); **and**

c) **a charge pump clock generating circuit** (see, *e.g.*, page 8 line 29-page 9 line 2, page 12 lines 4-26, and examples - 350 in Fig. 3, 500 in Fig. 5) **including a ring oscillator** (*e.g.*, page 12 lines 4-26, ref. 500) **comprising an odd number of not more than three inverting driver sections** (see, *e.g.*, page 12 lines 5-10 and examples - 508/502/514, 510/504516, 512/506/518 of Fig. 5) **cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section** (*e.g.*, 508/502/514) **is next after a last driver section** (*e.g.*, 512/506/518) **and one of the driver section outputs** (*e.g.*, 512/506/518 in Fig. 5) **constitutes a particular charge pump clock output** (see, *e.g.*, page 9 lines 26-29, page 10 lines 14-17, page 12 lines 23-25, and examples - 354, 356, 362 or 364, and 524) **controlling at least one of the transfer capacitor coupling switches** (see, *e.g.*, page 9 lines 26-29, page 12 lines 4-15, page 13 line 30-page 14 line 2, and examples - Fig. 5, paragraph 49; 602, 604, 608, or 610 of Fig. 6; 704 or 706 of Fig. 7; generally, switch circuits 800, 830 of Fig. 8 as used in Fig. 9 or Fig. 10), **and wherein each driver section includes**

i) **circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output** (see, *e.g.*, page 12 lines 5-15, and examples - 508, 510 and 512 of Fig. 5; exemplary details 426 of Fig.4), **and ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output** (see, *e.g.*, page 12 lines 5-15, and examples - 514, 516, 518 of Fig. 5, exemplary details 430 of Fig. 4);

d) **wherein the plurality of transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source** (see, *e.g.*, page 7 lines 3-21, page 13 line 30-page 14 line 16, page 16 line 27-page 18 line 3, and examples - +/- source connections 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via

524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times** (see, *e.g.*, page 12 line 27-page 13 line 2, and page 14 lines 17-28, paragraphs 51, 57).

V.A.2 Claim 43

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **by alternately transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10), **and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging switch circuit** (see, *e.g.*, page 12 line 31-page 13 line 2, page 16 line 27-page 18 line 3, and examples - 608 or 610 of Fig. 6; 706 of Fig. 7; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - 354, 356, 362 or 364 of Fig. 3, 524 of Fig. 5);

b) **limiting source current provided to each inverting driver** (see, *e.g.*, page 12 lines 5-8, and examples - 502, 504, 506 of Fig. 5) **output node of a current-starved ring oscillator** (*e.g.*, 500 of Fig. 5) **having not more than three inverting driver stages within a first charge pump clock generator circuit** (see, *e.g.*, page 12 lines 20-21, and examples - 350 of Fig. 3, 500 of Fig. 5) **by means of a corresponding source current-limiting circuit** (see, *e.g.*, page 12 lines 6-8 and examples - 508, 510, 512 of Fig. 5); **and**

c) **limiting sink current drawn from each of the inverting driver output nodes by the driver circuit by means of a corresponding sink current-limiting circuit** (see, *e.g.*, page 12 lines 8-10, and examples - 514, 516, and 518 of Fig. 5);

d) **wherein the inverting driver output node** (*e.g.*, 524 of Fig. 5) **of one** (506 of Fig. 5) **of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output.**

V.B Charge Pump Driven by a Substantially Sine-Like Generated Clock Output

Claim 12 (apparatus) and Claim 28 (method) are distinguished from the prior art in part by an output waveform that is distinct from waveforms of all previous integrated charge pump clock outputs, and which is contrary to the goals and practices of prior art charge pump design.

V.B.1 Claim 12

Charge pump apparatus within a monolithic integrated circuit for generating an output voltage supply (see, *e.g.*, page 7 lines 3-12, and examples: +/- outputs in Fig. 2 at 216/218 and/or 224/226, Fig. 3 at 316/318, Fig. 4 at 404/634, and Fig. 7 at 404/710; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9 as described from page 16 line 27 to page 18 line 3; and 1014/1016 in Fig. 10), **comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **coupled alternately between source connections** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **and output connections** (*e.g.*, references as previously noted for output voltage supply);

b) **a plurality of active switches** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10), **each switchable between a conducting state and a nonconducting state under control of at**

least one charge pump clock output (not shown in Fig. 2; see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Fig. 6, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10) **to couple charge, which is not substantially conducted by the charge pump clock output, from the source connections to the output connections;**

c) **a charge pump clock generating circuit** (see, *e.g.*, page 8 line 29-page 9 line 2, page 12 lines 4-26, and examples - 350 in Fig. 3, 500 in Fig. 5) **including an active driver circuit** (*e.g.*, 512/506/518 of Fig. 5) **configured to both source current to and sink current from the charge pump clock output** (524) **to cause a voltage waveform of the charge pump clock output to be substantially sine-like** (paragraph 50 at page 12, lines 16-26) **due to**

i) **circuitry** (see, *e.g.*, page 11 lines 22-25, page 12 lines 6-18, and examples - 512 in Fig. 5, exemplary details 426 in Fig. 4) **configured to limit source current provided by the active driver circuit to the charge pump clock output, and**

ii) **circuitry** (see, *e.g.*, page 11 lines 22-29, page 12 lines 8-18, and examples - 518 in Fig. 5, exemplary details 430 in Fig. 4) **configured to limit current sunk from the charge pump clock output by the active driver circuit.**

V.B.2 Claim 28

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **from a charge pump incorporated within a monolithic integrated circuit by transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS")** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13

line 7, page 13 lines 24-28, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10) **circuit is a switching circuit of the charge pump configured to couple the TC to a supply** (*e.g.*, source, output or intermediate; a supply has two terminals) **under control of a charge pump clock** (not shown in Fig. 2; see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Fig. 6, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10) **, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging TCCS circuit** (see, *e.g.*, page 12 line 31-page 13 line 2, page 16 line 27-page 18 line 3, and examples - [220 and 222] and/or [212 and 214] in Fig. 2; [312 and 314] in Fig. 3; [608, 610 and 616] in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (not shown Fig. 2; *e.g.*, 362 or 364 Fig. 3; 524 Figs. 6 and 7; 802 of Fig. 8 in Figs. 9 and 10); **and**

b) **actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions** (see, *e.g.*, page 12 lines 23-26, and examples - 512, 518 and 524 in Fig. 5) **such that a voltage of the first charge pump clock output is substantially sine-like** (paragraph 50, page 12 lines 16-26).

V.C Single-Phase Clock Coupled Passively without Transfer Current to TCCSs

It will be useful, first, to describe a distinction between two families of charge pumps, which reflects important differences in the function of the circuit identified as the "clock." The claims in this subsection cover only "control only" charge pumps, and do not cover "direct drive" charge pumps. Distinctions between these families, together with claim language establishing such distinction, are described in the following remarks.

"Control only" charge pump clock(s) provide only control signals to transfer capacitor coupling switches ("TCCSs"), which in turn convey the current to the transfer capacitor ("TC"), and do not provide significant current to the TC or the output. Examples of "control only" charge pumps include the Appellants' Figs. 2, 3, 6, 8 and 9, as well as Tasdighi (Figs. 2, 4, 7-9), Nork (Figs. 2A-9A), Bingham '774 (Figs. 1A, 1B and 3), Butler (Figs. 1-3) and Yokomizo (Figs. 1-5). At least one of each of the charge and discharge TCCSs is generally actively controlled by a clock output in a

"control only" charge pump, and often four TCCSs in a bridge are all actively controlled via their respective control nodes. Because the TCCSs in a "control only" charge pump are often arranged in a bridge around the TC, the term "bridge-type" is sometimes used to describe charge pumps of that topology.

"Direct drive" charge pump clocks conduct charge directly in order to generate the output supply. In fact, the capacitor coupled directly to such "clock" typically is the transfer capacitor. No TCCSs need appear to be "actively controlled" by a "direct drive" clock. Rather, the TCCSs are more commonly passive, similar to diodes or diode-connected FETs, reacting only to applied voltages to switch on (forward biased) or switch off (reverse biased). Examples of this family of charge pumps include Vaughn (Fig. 1; TCs 28, 40, 49, 53), Backes (Figs. 2-3, TCs C2, C3), Arakawa (Fig. 3, Co is TC) and Doluca (Fig. 3, TCs C1, C2), among others.

In a "direct drive" charge pump, TCCSs may appear to be passively, and indeed capacitively, coupled to the clock output. That is because the clock of such a charge pump performs the completely different function of providing current to the TC, rather than merely providing control signals to the TC. Due to this functional difference, comparison of "apples to apples" in charge pumps often requires cognizance of the family distinction. To avoid confusion, therefore, Claims 18 and 49 are limited to "control only" charge pumps. More explicitly, they are restricted to clocks that do not directly provide significant current to the TC or to the output.

V.C.1 Claim 18

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) **one or more source switching devices** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig.

9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to convey transfer current to the transfer capacitor from the voltage source when conducting;**

c) **one or more output switching devices** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **disposed in series between the transfer capacitor and the output voltage supply to convey transfer current from the transfer capacitor to the output voltage supply when conducting; and**

d) **a charge pump clock generating circuit** (*e.g.*, 500 in Fig. 5) **configured to provide a single-phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10) **coupled passively** (exclusively via passive devices, see, *e.g.*, page 13 line 30-page 14 line 12, page 16 lines 12-13, and examples - 618 and 620 in Fig. 6, 812 for switches 800 in Figs. 9-10) **without conveying substantial transfer current** (*i.e.*, not a direct-drive clock), **to control nodes** (*e.g.*, FET gates, isolated from TCs) **of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively** (*e.g.*, via 622 and 624 of Fig. 6, or 822 of switches 830 in Figs. 9-10), **without conveying substantial transfer current, to control nodes** (FET gates, isolated from TCs) **of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.**

V.C.2 Claim 49

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit by alternately transferring charge from a**

voltage source (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10), **and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a TC discharging switch** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a single phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10) **that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC** (not shown Fig. 2; see, *e.g.*, page 13 lines 24-29, and examples - capacitors 622 and 624 to gates of FETs 608 and 610, respectively, in Fig. 6; capacitors 812 to gates of FETs 808, or capacitors 822 to gates of FETs 818 of Fig. 8 for Figs. 9-10); **and**

b) **coupling the TC to the voltage source via a TC charging switch** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10), **during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch** (not shown Fig. 2; coupled exclusively via passive devices, see, *e.g.*, page 13 line 30-page 14 line 12, page 16 lines 12-13, and examples - 618 and 620 in Fig. 6, 812 for switches 800 in Figs. 9-10, to control nodes such as a gate of FET 602 or FET 604 in Fig. 6, and a gate of a FET 818 or a gate of a FET 808 of Fig. 8 for Figs. 9-10).

V.D Claim 21: Discharging Switch Device Area Disparity

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a circuit, comprising:**

a) a transfer capacitor ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) one or more source switching devices (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10);

c) a first output switching device (see, *e.g.*, page 13 lines 3-16, and examples - FET 314 of Fig. 3, FET 610 of Fig. 6) **having a first device area disposed between a first terminal** (*e.g.*, right side of 202 in Fig. 3, right side of 606 in Fig. 6) **of the transfer capacitor and the output voltage supply** (*e.g.*, Vo- 318 of Fig. 3, Vo- 634 of Fig. 6), **and a second output switching device** (see, *e.g.*, page 13 lines 3-16, and examples - FET 312 of Fig. 3, FET 608 of Fig. 6) **disposed between a common reference connection** (*e.g.*, Vo+ 316 of Fig. 3, common 404 of Fig. 6) **of the output voltage supply and a second terminal** (*e.g.*, left side of 202 in Fig. 3, left side of 606 in Fig. 6) **of the transfer capacitor opposite the first terminal of the transfer capacitor, having a second device area that is greater than double the first device area; and**

d) a charge pump clock generating circuit (see, *e.g.*, page 12 lines 27-28 *et seq.*, and example 500 of Fig. 5 for 524 of Fig. 6, or for 802 of Figs 7 and 8 as used in Figs. 9 or 10) **configured to provide a single-phase charge pump clock output coupled to all of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled to all of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices.**

V.E Clock Coupled Capacitively to an Isolated Control Node of a TCCS

This preferred coupling technique solves several problems of implementation.

V.E.1 Claim 24

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **for conveying charge from a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to the output voltage supply;**

b) **one or more source switching devices** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;**

c) **one or more output switching devices** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node** (not shown Fig. 2; see, *e.g.*, page 13 lines 24-29, and examples - gates of FETs 608 and 610 in Fig. 6; gates of FETs 808 or FETs 818 of Fig. 8 for Figs. 9-10) **that is substantially isolated from both the transfer capacitor and the voltage source** (unlike, *e.g.*, gates of 704 and 706 in Fig. 7); **and**

d) **a capacitive coupling circuit** (see, *e.g.*, page 13 line 30-page 14 line 1, and examples - 618/626, 620/628, 622/630 and/or 624/632 in Fig. 6; 812/810 and/or 822/820 in Fig. 8 for Figs. 9-10) **coupling a charge pump clock output** (*e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10) **to one of the control nodes corresponding to a source switching device** (whether or not referred to in (b)) **or to an output switching device** (whether or not referred to in (c)).

V.E.2 Claim 60

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit by alternately transferring charge for the output from a source voltage** (see, *e.g.*, page 7 lines 3-21, page 12 lines 27-31, page 16 line 27-page 18 line 3, and examples - +/- source connections 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10)**, and from the TC to the output supply, the method comprising:**

a) **coupling a first charge pump clock output** (*e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10) **to a control node** (see, *e.g.*, page 13 lines 24-29, and examples - gates of switching FETs) **of a TC charging switch** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **via a first capacitive coupling network that does not conduct a significant portion of the charge for the output** (see, *e.g.*, page 13 line 30-page 14 line 12, page 14 lines 29-31, R*C product preferably about 10*period of clock, hence insignificant current, and gates are isolated from TC and supply; and examples - 618/626, 620/628, 622/630 and/or 624/632 in Fig. 6; 812/810 and/or 822/820 in Fig. 8 for Figs. 9-10);

b) **coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output** (see, *e.g.*, page 7 lines 3-21 and page 12 lines 27-31;

c) **coupling a second charge pump clock output** (may be like 350 of Fig. 3 in having plural outputs or phases, so may be another or the same of, *e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10,) **to a control node** (*e.g.*, gate of switching FET) **of a TC discharging switch** (see, *e.g.*, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - 312 and/or 314 in Fig. 3; 608 and/or 610 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 800 in Fig. 10) **via a second capacitive coupling network** (see, *e.g.*, page 13 line 30-page 14 line 12, and examples - 622/630 and/or 636/638/624/632 in Fig. 6; 822/820 or 812/810 in Fig. 8 for Figs. 9-10) **that does not conduct a significant portion of the charge for the output** (see, *e.g.*, page 14 lines 29-31, R*C product preferably about 10*period of clock, hence insignificant current, and gates are isolated from TC and supply, hence insignificant current); **and**

d) **coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output** (see, *e.g.*, page 7 lines 3-21, page 12 line 31-page 13 line 2, page 16 lines 16-29-page 17 lines 17-19).

V.F Claim 42: Switch AC Impedance Disparity with Clock dV/dt Limit

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **from a charge pump by transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, page 15 lines 17-27, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10) **is a switching circuit of the charge pump configured to couple the TC to a supply** (any of the supplies noted above, or a further one such as

represented in Fig. 9) **under control of a charge pump clock** (*e.g.*, 354, 356, 362 and/or 364 of Fig. 3; 524 of Fig. 6) **, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging TCCS circuit** (see, *e.g.*, page 10 lines 1-9, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - FETs 312 and/or 314 of Fig. 3; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (*e.g.*, 364 or 362 of Fig. 3, or 524 of Fig. 6);

b) **actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions** (see, *e.g.*, page 12 lines 4-26, and examples - current sources 512 and 518 of Fig. 5);

c) **coupling a first terminal** (*e.g.*, left side of 202 of Fig. 3 or 606 of Fig. 6) **of the TC to a common reference connection of the output supply** (*e.g.*, Vo+ 316 of Fig. 3, 404 of Fig. 6) **via a discharge common TCCS** (*i.e.*, a TCCS for discharging a TC to said common reference connection, see, *e.g.*, page 13 lines 3-16, and examples - FET 312 of Fig. 3, FET 608 of Fig. 6);

d) **coupling a second opposite terminal** (*e.g.*, right side of 202 of Fig. 3 or 606 of Fig. 6) **of the TC to an output supply connection** (*e.g.*, Vo- 318 of Fig. 3; Vo- 634 of Fig. 6) **opposite the common reference connection via a discharge output TCCS** (*e.g.*, FET 314 of Fig. 3; FET 610 of Fig. 6); **and**

e) **fabricating the discharge output TCCS to have a control node AC impedance** (see, *e.g.*, paragraph 52, page 13 lines 3-16) **at least double a control node AC impedance of the discharge common TCCS.**

V.G Claim 52: Discharging Switch AC Impedance Disparity

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **by alternately transferring charge from a voltage source** (see, *e.g.*, page 7 lines 3-12, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10), **and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches** (see, *e.g.*, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - FETs 608 and 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of the single phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10);

b) **coupling the TC to the voltage source via a TC charging switch** (see, *e.g.*, page 12 lines 29-31, and examples - 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10), **during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output;**

c) **coupling a first TC discharging switch device** (*e.g.*, 608 of Fig. 6) **in series between a first node of the TC** (*e.g.*, left side of 606 in Fig. 6) **and a common reference connection** (*e.g.*, 404 of Fig. 6) **of the output supply;**

d) **coupling a second TC discharging switch** (*e.g.*, 314 of Fig. 3 or 610 of Fig. 6) **in series between a second node of the TC** (*e.g.*, right side of 202 in Fig. 3; or right side of 606 in Fig. 6) **opposite the first node and a connection of the output supply** (Vo- 318; or Vo- 634 of Fig. 6) **opposite the common reference connection; and**

e) **fabricating the second TC discharging switch to have a control node AC impedance** (see, *e.g.*, paragraph 52, page 13 lines 3-16) **at least twice as large as a control node AC impedance of the first discharging switch.**

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented for review:

Whether Claim 18 is unpatentable as anticipated under 35 USC 102(b) by Tasdighi.

Whether Claims 1-4, 10, 12, 14, 16, 19-20, 28-33, 36, 40, 43-44, 48-51, 53-54 and 57-58 are unpatentable as obvious under 35 USC 103(a) over Tasdighi in view of Yamauchi.

Whether Claims 1-9, 12, 14-18, 20, 22, 24-41, 43-51, 53-61 and 66-67 are unpatentable as obvious under 35 USC 103(a) over Tasdighi in view of Hara.

Whether Claims 1-10, 12-20, 22-25, 27-41, 43-51, 53-61 and 66-67 are unpatentable as obvious under 35 USC 103(a) over Tasdighi in view of Ito.

Whether Claims 10, 12-15, 19-21, 27-28, 34-36, 39, 41-43, 45-48, 50-53, 56, 60, 62-63 and 65-66 are unpatentable as indefinite under 35 USC 112, second paragraph.

VII. ARGUMENT

The Appellants regret the extreme length of this Appeal Brief. No restriction requirement was issued, leaving 65 claims at issue in this appeal. Moreover, the Examiner has set forth three nearly identical, overlapping grounds of rejection for most of the 65 claims at issue, asserting Tasdighi first in combination with Yamauchi, then with Hara, and then with Ito. The three secondary references are very similar, similarly failing to disclose required elements of the Appellants' claims that are missing from Tasdighi. Because no further argument will be permitted in this appeal, each and every rejection is thoroughly addressed is this Appeal Brief.

The numerous grounds of rejection set forth by the Examiner are improper for various reasons, but the panel is respectfully requested to particularly note certain systematic errors that the Examiner makes repeatedly: in particular, asserting that a reference teaches or fairly suggests a particular feature based not on the presence of the asserted feature in the cited reference, but on the absence of contrary teaching. Some of these errors are briefly set forth in summary form below.

SUMMARY OF MOST SIGNIFICANT EXAMINATION ISSUES

This section provides a summary of issues that are each common to a multiplicity of claims. The Appellants respectfully submit that each issue describes a highly pertinent, systematic error that is repeatedly made by the Examiner. Because many of the individual claim rejections rely on the improper methodology described below, these few issues provide sufficient grounds to reverse the Examiner as to most of the outstanding rejections. Thus, considerable time may be saved by reviewing this summary in conjunction with analysis of the individual rejections. Moreover, understanding of these errors should result in improved examination in the future.

ASSERTING FEATURES NOT IN EVIDENCE

The Examiner rejects a number of claims as anticipated or obvious using the following process to justify such rejection. First, the Examiner properly identifies features of the claim that are present in the cited prior art. Then, as to one or more features of the claim that are not taught or

disclosed by the cited references, the Examiner asserts, without evidence for support, that such feature "could have" been included or used in the prior art. He then relies upon such undisclosed feature as a basis for rejecting a claim, arguing that this is proper because the prior art provides no evidence that the undisclosed feature was not, in fact, as the Examiner asserts it could have been.

Examples: In respect of Claim 19, the Examiner states (Final Rejection, page 19 beginning line 7, underlining added for emphasis):

> Although the reference(s) read on the limitations of claims 18 and 49 as previously described above, the reference(s) do not show or disclose a second charge pump stage of claim 19, or second TC, second TC charging switch, second output supply, and second TC discharging switch of claim 54. However, it would have been obvious to one of ordinary skill in the art to add a second charge pump stage/apparatus to the charge pump apparatus of claim 18, or add the elements related to the method steps of claim 49. It could have the same basic structure as Tasdighi's Fig. 2, wherein the second charge pump stage could be coupled in parallel to the charge pump apparatus, and both would receive the same charge pump clock output.

The Examiner's conjecture as to what the prior art might have taught is quite explicit in this example.

In rejecting Claim 18, the Examiner similarly conjectures as to what the cited prior art teaches. In this example, rather than stating that the feature "could have been" as required by the claim, the Examiner states that the device features are "considered as being" as required by the claim. As described in more detail below, the Examiner cites the Tasdighi '291 reference in rejecting Claim 18, and specifically Figs. 2-3 of this reference. Specifically, the Examiner states (Final Rejection, page 13 beginning line 20; underlining added, bracketing in original):

> Since the charge pump clock output of oscillator 24 is not shown with any intervening elements between it and the control nodes of each switch SW1, SW2 (i.e., switching devices 26 and 27), the single-phase charge pump clock output is considered as being coupled passively to the control nodes of the switching devices. [Note: A signal line is considered one type of a passive element, that can have parasitic capacitive, or inductive, characteristics related to the line.] Since the clock output is coupled to the gates of MOS transistors 26 and 27, even if they do have some leakage current associated within them, there will be no substantial transfer current conveyed, and claim 18 is anticipated.

As described in detail below, the Tasdighi '291 figures show no more than an arrow pointing between blocks, or an unconnected "Control" line. As admitted by the Examiner, no intervening elements are shown between the oscillator and the control nodes of each switch. Thus, Tasdighi is silent with regard to many of the electrical details required by Claim 18. For example, Tasdighi teaches no details regarding a coupling between a single-phase charge pump clock output and control nodes of source switching devices. However, despite this lack of teaching of Tasdighi, the Examiner asserts that the clock output is considered as being passively coupled as required by Claim 18. Not only is the Examiner's assertion unsupported by the disclosure of Tasdighi, which does not show any detail of such coupling, but it is, in fact, contrary to the evidence of all other prior art, as demonstrated at length in the remarks of sections VII.A.1.c and VII.A.1.d.

The examples set forth above are not isolated instances. Rather, the Examiner frequently uses such conjecture as a basis for rejection, and has actively defended its use in discussions preceding and during this appeal. With regard to a claimed feature not shown or suggested in a prior art reference, the Examiner has rejected several claims by simply asserting that the claimed feature could be present in the prior art reference. The Examiner defends this approach by stating that nothing in the reference precludes the possibility that the claimed feature might be present in the prior art reference. His statement does not make literal sense: the claimed feature is manifestly not present in the reference now, and such absence certainly precludes it being present. However, it is believed that the Examiner means that the claimed element could have been a part of a circuit that is represented by an illustration in the reference, which illustration was, however, simplified by omitting such detail.

The Appellants respectfully submit that any rejection relying upon such *absence of contrary subject matter* in lieu of the required *presence* of claimed subject matter is contrary to settled law, and should be promptly reversed. *Prima facie* obviousness requires each claimed feature to be disclosed in the combined references in as much detail as claimed, just as in anticipation. "The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)

(endnote 2). The fact that the Examiner needs to state that a circuit described by a reference "could have" included a claimed feature amounts to an admission that the reference itself *does not* include such feature, and thus is effectively an admission that the foregoing requirement is *not* met by the cited prior art.

Basing rejections on the grounds of a feature that *is not*, but "could have been" a tacit part of a prior art reference, would turn on its head the legal requirement for *prima facie* obviousness of a claim, by requiring an applicant to prove that the prior art "could not have" contained the missing subject matter. Demonstrating that cited prior art discloses each of the features required by a claim requires a showing of evidence of each feature. The required showing of evidence is not met by merely stating that such a feature is not precluded by the prior art.

If such an examination approach were permitted under the patent laws, instead of requiring an examiner to demonstrate that the prior art discloses each claimed element in as much detail as claimed in support of *prima facie* obviousness (citations), applicants would be required to prove that the prior art "could not have" contained the claimed elements. Under such an approach, the examiner would need only conjecture that the prior art "could have" employed the asserted feature. In the absence of actual evidence of the asserted feature, such conjecture is necessarily based on the rejected claim itself, impermissibly relying on hindsight.

The unfairness of basing rejections on what the prior art "could have" disclosed has elicited sharp rebukes of such rejections by reviewing judges. Consider, for example, the impatience reflected in this acerbic passage (emphasis in original): "That one *could* invent such a cable tie is unquestioned. Caveney *did*. The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made." *Panduit Corporation V. Dennison Manufacturing Co.*, 774 F.2d 1082, 1092, 227 U.S.P.Q. 337, 347 (Fed Circuit, 1985)(endnote 8).

Although doctrines such as "inherency" and "common knowledge" provide exceptions whereby a feature not in evidence may be considered to be present in a prior art reference, the exceptions are narrow, and do not apply to the present circumstances (*see* section VII.A.1.f "Other Doctrines for Asserting Missing Descriptive Material are Also Unavailing"). In any event, the

Examiner does not assert any such exceptional doctrine to justify his reliance on conjecture to support several different grounds for rejection. The Appellants earnestly request the panel to reverse each rejection that relies upon such conjecture, including Claims 18-20, 22-23, 49-51, and 53-59.

IGNORING CONTRARY EVIDENCE

MPEP 2143.01 includes a bold, capitalized subheading stating "Where the teachings of the prior art conflict, the examiner must weigh the suggestive power of each reference," citing *In re Young*. A similar proposition, that contrary evidence must be considered, is supported in this Brief by *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert denied*, 469 U.S. 851 (1984)(endnote 6). *W.L.Gore* is relied upon because the facts in that case are closely analogous to facts in this Appeal, as described in detail in subsection VII.B.1.a "Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi." *W.L.Gore* requires consideration of contrary evidence, especially when strong positive evidence is lacking, clearly supporting the admonishment of MPEP 2143.01. Despite an absence of clear evidence of required features, the Examiner consistently fails to consider contrary evidence indicating that such features are not fairly taught by the prior art.

As a first example, Independent Claims 1 and 43 each include a limitation requiring a ring oscillator having not more than three driver sections (stages). Three grounds of rejection are outstanding for these claims. For the three-section ring oscillator, one ground relies on Yamauchi, a second on Hara, and the third on Ito. None of these references discloses the required limitation. Tasdighi has no information at all about specifics of ring oscillators. Yamauchi describes ring oscillators for a charge pump having an "odd number" of stages, and moreover represents such ring oscillators with illustrations that actually include only 3 driver sections (Figs. 6 and 7). However, the illustrations use three dots " ... " between stages to show that further stages are being omitted, and thus these figures cannot be fairly taken to indicate three sections in a ring oscillator used for a charge pump. Ito describes ring oscillators for Voltage Controlled Oscillators; however, while the Appellants acknowledge that three-stage ring oscillators are known and are useful for some purposes, the combination requires that such oscillators to be used to drive a charge pump. The evidence might therefore be ambiguous, except for two things: in the crowded field of charge pumps,

no examples of three-stage ring oscillators for charge pumps have been found despite arduous searching. Even more crucially, Hara teaches explicitly that ring oscillators for charge pumps should have at least five sections (see col. 5 lines 60-62). These two facts are contrary to the contention of the Examiner, and should be acknowledged as resolving any ambiguity in favor of a conclusion that the prior art does not teach the use of three-stage ring oscillators, especially current-starved ring oscillators as required, for use with charge pumps.

As a second example, independent Claim 18 is rejected as anticipated by Tasdighi, while independent Claim 49 is rejected over Tasdighi in view of Ito, and again in view of Yamauchi. Both claims require a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of [each charging switch and each discharging switch]. In each case, the Examiner relies upon Tasdighi for disclosure of the noted requirement. As noted above, Tasdighi lacks the details relied upon by the Examiner; the evidence is not merely ambiguous, it is entirely absent. Worse, Tasdighi incorporates by reference a further patent, US 4897774 to Bingham et al. ("Bingham '774," *see* col. 3 line 44 - col. 4 line 16), identifying it as the basis for Fig. 4. Bingham shows circuit details that are omitted in Tasdighi. The details revealed in Bingham demonstrate that the source of the illustrations in Tasdighi was contrary to the claimed feature. In particular, Bingham shows that the actual system uses a plural-phase clock and active coupling to the charging and discharging switches. Thus, the Examiner's conjecture as to the circuit that Tasdighi "could have" used is not only wholly unsupported by evidence, it is moreover contrary to the evidence.

In each example, evidence in support of the Examiner's assertion is, at the most, ambiguous, and in each example any remaining question is properly resolved in favor of allowability by proper consideration of evidence that is contrary to the Examiner's assertion. As such, each rejection of independent Claims 1, 43, 18 and 49, as well as all depending therefrom, should be promptly reversed.

REFUSAL TO CREDIT THE PLAIN MEANING OF A CLAIM TERM

A claim term must be construed in accordance with its plain meaning, unless the Applicants clearly indicate a contrary intent (citations in support of this well known proposition are set forth below).

Independent Claims 12 and 28, all claims depending therefrom, and various other dependent claims, all require charge pump clock output that is "substantially sine-like" due to [active limiting circuitry]. The Examiner points to no evidence that the prior art teaches a charge pump clock output that is even *remotely* sine-like. To the contrary, all of the numerous references of record are shown to have square or near-square waveforms. A "sine" has a precisely defined mathematical shape, and thus "substantially sine-like" is a waveform which, while not precisely a sine, nonetheless is at least generally like a sine, which is clearly different from all prior art of record. The Examiner refuses to credit the plain meaning of "sine," suggesting that any alternating waveform could be called "substantially sine-like." The Examiner objects to the absence of a waveform illustration in the application. However, waveforms are only examples, and are less able to establish the precise boundary of a "sine-like" waveform than is the succinct statement that the waveform is substantially sine-like. By its plain meaning, the claim term merely provides a "penumbra" around a precisely defined waveform, and is thus readily understood by those of skill in the electronics arts.

Numerous other issues are described in detail in this Amended Appeal Brief, and are not less important or less valid for not being mentioned in this SUMMARY OF MOST SIGNIFICANT EXAMINATION ISSUES. However, the issues noted herein provide ample grounds for reversing most of the outstanding rejections. As such, this SUMMARY OF MOST SIGNIFICANT EXAMINATION ISSUES serves as an efficient introduction to this Amended Appeal Brief.

The detailed arguments are set forth below.

VII.A. Rejections Under 35 USC § 102

VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi

Claim 18 stands rejected by the Examiner under 35 USC 102(b) as anticipated by Tasdighi. This ground of rejection is traversed because Tasdighi fails to disclose a multiplicity of elements

required by Claim 18. The failure of the Examiner to properly support this ground of rejection is sufficiently demonstrated by the following subsections *VII.A.1.a Missing Descriptive Matter* and *VII.A.1.b Literal Disclosure of Tasdighi versus Disclosure Attributed by the Examiner*. However, the Examiner engages in substantial speculation as to what might be shown in Tasdighi. Therefore, considering that Tasdighi arguably refers to the prior art for details, the relevant teaching of all prior art of record is also set forth below. Subsections *VII.A.1.c Disclosure of Tasdighi that is Incorporated by Reference* and *VII.A.1.d Disclosure of Coupling in "Control Only" Charge Pumps in Prior Art of Record* describe such prior art.

VII.A.1.a Missing Descriptive Matter

Claim 18 recites in part (underlining added for emphasis):

> [A] charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.

Tasdighi fails to disclose or fairly suggest each of the multiplicity of elements of Claim 18 that are underlined above, which together will be referred to as "the missing descriptive matter," thereby precluding anticipation under 35 USC §102(b). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)[1]. Moreover, each feature must be disclosed in as much detail as is claimed. "The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)[2].

The remarks set forth below require a conclusion that Tasdighi entirely fails to satisfy the foregoing legal requirements with respect to the missing descriptive matter. To support this conclusion, three sources of disclosure by Tasdighi are analyzed: (1) literal disclosure within the pages of Tasdighi; (2) the disclosure of a related patent that is incorporated by reference in Tasdighi; and (3) the state of charge pump art prior art, as reflected in the prior art of record. As set forth below, the missing descriptive matter is absent from the literal disclosure of Tasdighi, is not supported by the material incorporated by reference, and is contrary to the practice of those skilled in the art as reflected in the prior art of record. The rejection refers only to the direct (literal) disclosure of Tasdighi, and hence the Examiner's reasoning is set forth and traversed in the section below.

VII.A.1.b Literal Disclosure of Tasdighi versus Disclosure Attributed by the Examiner

In rejecting Claim 18 under §102(b), the Examiner points to Figs. 2 and 3, and to column 3, lines 16-36 and 37-43, of Tasdighi. Fig. 2 shows a block 24 "OSC," with an arrow pointing from the block 24 to a different, unnumbered block that contains simplified mechanical representations SW1 and SW2 instead of actual charge pump circuit details. Column 3 lines 16-19 recite in part: "An oscillator 24 ... produces a train of pulses which are applied to control terminals of switching transistors SW1 and SW2." [Note the imprecision of this description: SW1 and SW2 are not transistors, but are mechanical representations of switch functions, requiring at least pairs of transistors for implementation.] The remainder of the paragraph, to line 36, describes charge pump switching operation as a sequence of on/off conditions, as if the switches were ideal, yet "under control of oscillator 24" (lines 24-25). None of the material cited by the Examiner literally describes any of the missing descriptive matter, or indeed provides any switch control detail at all.

However, lines 37-43 of the cited reference continue: "Switches SW1 and SW2 may each be a conventional CMOS inverter as shown in Fig. 3, comprising an NMOS transistor 26 and a PMOS transistor 27. As the oscillator 24 voltage applied to the gates of transistors 26 and 27 alternates between a high a low voltage, transistors 26 and 27 couple either a V_A voltage or a V_B voltage to the output of the CMOS circuit." The Examiner primarily relies upon this description as disclosing the missing descriptive matter. The Examiner's reliance is misplaced, because this description fails to

literally describe any of the missing descriptive matter of Claim 18 as indicated above by underlining.

The following passage of the Final Rejection show that the Examiner acknowledges that Tasdighi does not actually teach the clock output (to prove that it is single phase), nor the connections to each of the charge switches and each of the discharge switches. The bracketed note is present in the original Final Office Action, but underlining is added to underscore the reasoning by which the Examiner attributes the missing descriptive matter to Tasdighi (beginning at page 13, line 20 of the Final Office Action; underlining added, bracketed material in original).:

> Since the charge pump clock output of oscillator 24 is not shown with any intervening elements between it and the control nodes of each switch SW1, SW2 (i.e., switching devices 26 and 27), the single-phase charge pump clock output is considered as being coupled passively to the control nodes of the switching devices. [Note: A signal line is considered one type of a passive element, that can have parasitic capacitive, or inductive, characteristics related to the line.] Since the clock output is coupled to the gates of MOS transistors 26 and 27, even if they do have some leakage current associated within them, there will be no substantial transfer current conveyed, and claim 18 is anticipated.

The Examiner's rejection is based on conjecture rather than on evidence. As may be seen by the Examiner's assertion above, the Examiner explicitly bases his conclusions on that which is not shown in Tasdighi. His conjectures include: (i) that Tasdighi's clock is single phase; and (ii) that the coupling between the clock and the switching elements is passive. His rationale for attributing these conjectured conclusions to Tasdighi is based on the absence of electrical circuitry details. Thus, for example, the Examiner submits that the absence of "intervening elements" justifies ("considered as being") a conclusion that the charge pump clock output is passively coupled to the control nodes are passively coupled. However, there are no intervening elements in the figures only because there are no elements whatsoever indicating details of the coupling. The complete lack of disclosure of these features could not be clearer.

The use of a single non-electrical arrow from the oscillator block 24 is also insufficient, for the same reason, to support a conclusion that Tasdighi fairly suggests a "single phase oscillator." No

electrical information is provided, and hence no electrical conclusions may be drawn from the literal disclosure of Tasdighi. Unlike the specified coupling details, it is true that many charge pumps use a single-phase clock. However, those prior art references that use a "control only" charge pump architecture, such as that illustrated in Tasdighi, invariably employ active coupling to essentially generate a plural-phased clock.

The Examiner's statement (emphasis added) that the clock output "is considered as being coupled passively to the control nodes of the switching devices" is conjecture that is entirely unsupported by evidence, whether in Tasdighi, in documents incorporated by reference in Tasdighi, or in the prior art of record. His reasoning is based, instead, on an absence of contrary evidence, as his words acknowledge: "Since the charge pump clock output of oscillator 24 is not shown with any intervening elements between it and the control nodes of each switch ... ." The simple fact is that Tasdighi does not show or describe the detail required by the claim. That fact is directly contrary to the legal standard, articulated above in *Richardson* (*id.*, endnote 2), that anticipation requires that "[t]he identical invention must be shown in as complete detail as is contained in the patent claim." The actual evidence supporting the Examiner's conclusion thus clearly fails to meet the requirements for anticipation. As such, Tasdighi fails to anticipate Claim 18, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection.

However, the Appellants have set forth below substantial further evidence demonstrating that the Examiner's assertions as to the disclosure of Tasdighi are not only unsupported by the actual disclosure of Tasdighi, but are moreover contrary to the practices of those skilled in this art.

VII.A.1.c Disclosure of Tasdighi that is Incorporated by Reference

Tasdighi incorporates by reference a further patent, US 4897774 to Bingham et al. ("Bingham '774," *see* col. 3 line 44 - col. 4 line 16), which Tasdighi credits as the source of Fig. 4 shown in Tasdighi (col. 3 lines 45-47). Both Figs. 2 and 4 of Tasdighi (as well as Figs. 1A, 1B and 3 of Bingham '774) illustrate charge pumps having a "control only" architecture. (See subsection *V.C Single-Phase Clock Coupled Passively without Transfer Current to TCCSs* for explanation of "control only" versus "direct drive" charge pumps. Briefly, the distinction lies in the use of the charge pump clock: "direct drive" charge pump clocks directly drive transfer current into the transfer

capacitor, while clocks in "control only" charge pumps provide switch control only, and do not provide substantial current to the transfer capacitor.)

Tasdighi indicates the similarity of the charge pumps of Figs. 2 and 4 (*e.g.*, col. 4 lines 17-18, 19-22, and 26-27). Because Fig. 1A of Bingham '774 is identical to Fig. 4 of Tasdighi, and because Tasdighi fails to disclose electrical details of charge pump clock-to-switch coupling, it is logical to look to Bingham '774 as the most likely source of teaching of implementation details such as coupling. The Examiner did not turn to Bingham '774 for examples of coupling details; the details provided there are contrary to the requirements of the missing descriptive matter and contrary to the Examiner's conclusions cited above.

Fig. 1B of Bingham '774, in conjunction with Fig. 2, illustrates coupling details between a clock (OSC. 56 in Fig. 2) and the switches of a charge pump. The clock OSC 56 is coupled directly to FETs 44, 46, 48 and 50, and indirectly to FETs 52 and 54. The output of Fig. 2 is shown as phases 44 and 46; in Fig. 1B, the entire clock and inversion circuit is illustrated as "Φ CONTROL" 42 having output phases 44 and 46. The two output phases 44 and 46 control all of the bridge switches of both stages of the charge pump, but note that each stage employs both phases to control the switches.

Bingham '774 may be considered either as having a single-phase clock 56 that is actively coupled to the bridge switches of the charge pump via the FETs of Fig. 2, or else it may be considered as having a two-phase clock 42 that is directly coupled to the bridge switches of a charge p ump. There is no ambiguity when comparing the circuitry of Bingham '774 to that claimed in the Appellants' Claim 18, because Claim 18 requires both a single-phase clock and passive coupling. Both limitations are recited precisely due to the interchangeability of such terminology. Bingham '774 clearly fails to provide the missing descriptive matter indicated for Claim 18, and thus fails to support the Examiner's conjecture in this regard.

Relying on conjecture for circuit details to support a rejection of a claim is never appropriate, but it is egregiously inappropriate in view of the ample details incorporated into Tasdighi by reference to Bingham '774, and is made yet worse by the fact that the actual material of Tasdighi (including Bingham '774) contradicts such conjecture.

VII.A.1.d Disclosure of Coupling in "Control Only" Charge Pumps in Prior Art of Record

Tasdighi Figs. 2-4 merely reflect the Prior Art, and the prior art of record fails to support the Examiner's conjecture as to what Figs. 2-4 *could* represent. Each of Figs. 2-4 is labeled with the legend "Prior Art." As such, these figures cannot properly be construed in a manner contrary to the prior art. However, the Examiner's conjecture as to the content of Tasdighi's missing descriptive matter in these "Prior Art" figures is unsupported by the prior art of record. A survey of the prior art of record is set forth below to support this conclusion.

To avoid confusion, it is important to clearly distinguish two different families of charge pumps. Subsection *V.C Single-Phase Clock Coupled Passively without Transfer Current to TCCSs* describes the distinction in detail, and is incorporated here by reference for that purpose. The analysis set forth immediately below addresses only "control only" charge pumps (which satisfy the Claim 18 requirement "... clock output coupled passively, without conveying substantial transfer current, to control nodes of "[source and sink TCCSs]". To avoid conjecture, the following analysis also addresses only those references that include sufficient detail to definitively determine whether or not they accord with Claim 18.

All coupling details in the prior art of record are contrary to the Examiner's conjecture, and contrary to the requirements of Claim 18. In telephonic discussions, the Examiner acknowledged that Tasdighi does not illustrate details of the clock-switch coupling. He lamented that "many references fail to illustrate coupling details," but nonetheless insisted that such absence of detail could properly be interpreted as evidence of the claimed combination of coupling features recited in Claim 18. The following examples prove that appropriate details are before the Examiner, having only the drawback of failing to conform to his conjecture.

Thirty-two prior art references are of record in this appeal, as listed and numbered in section **IX. Evidence Appendix**. Of these, the following US patents describe "control only" charge pumps, together with sufficient information to ascertain whether they are consistent with the Examiner's conjecture as to the missing descriptive matter of Tasdighi (with numbering from Evidence Appendix):

2. U.S. Patent No. 6,411,531, issued 6/25/02 to Nork, et al. ("Nork")

3. U.S. Patent No. 6,518,829, issued 2/11/03 to Butler ("Butler")

11. U.S. Patent No. 6,400,211, issued 6/4/02 to Yokomizo, et al.

18. U.S. Patent No.4,777,577, issued 10/11/88 to Bingham, et al.

19. U.S. Patent No.4,897,774, issued 1/30/90 to Bingham, et al.

References 18 and 19 are believed to have substantially identical specifications, both being continuations of the same patent application. Moreover, reference 19 is the Bingham '774 reference that is shown in the immediately preceding section to teach coupling contrary to the claimed limitations. Thus, references 2, 3 and 11 constitute all of the references of record that have sufficient information and are relevant to "control only" charge pumps, and which have yet to be analyzed.

Nork clearly teaches "control only" charge pumps as Prior Art in each of Figs. 1A, 2A and 3A (transfer capacitor 8, switches 1-4 represented using mechanical switch symbol). The oscillator (18 or 25) explicitly outputs two different phases, V_{CLK} and V_{CLKB}, which are shown in Fig. 3B to be generally inverse to each other, with non-overlapping "high" states. Fig. 4A includes some circuit details: S1 and S2 are still represented as ideal mechanical switches, while switches 3 and 4 are detailed as FETs 46 and 44, respectively. As may be seen in the details of Fig. 4A, both phases of the oscillator 25 are used to control the latter two switches, and both phase signals are coupled to the controlled bridge switch via active circuitry. Fig. 8A is a simplified schematic of a 2-stage "control only" charge pump which uses two phases from oscillator 25 to control two of the bridge switches for each stage. Both phases are coupled to the bridge switch FETs via active circuitry. The remaining illustrations of Nork are consistent, but are simplified by omitting details. Note that both clock phases are clearly square wave signals (see Figs. 3B, 6B and 8B).

Butler illustrates a "control only" charge pump in Figs. 2 and 3 that employs transfer capacitor 64 and FETs 52, 54, 58 and 60 as bridge switches. (Fig. 1 is generally similar prior art). Each illustration explicitly identifies a multiplicity of different clock phases, all of which are square wave signals that are coupled to the controlled bridge switches via active circuitry.

Yokomizo Fig. 1 shows a "control only" charge pump including transfer capacitor C1 and idealized bridge switches SW1-SW4. The oscillator is not clearly shown to be single phase, but is

clearly shown to be actively coupled to SW3-SW4 via an inverter. Each of Figs. 2-5 also includes a nearly identical charge pump stage, driven similarly; Figs. 3 and 4 add second stages that are substantially the same. In each charge pump stage, the oscillator is actively coupled to at least some of the bridge switches.

These three references post-date Tasdighi, and thus are not prior art with respect to Tasdighi. Nonetheless, they represent the practice of those skilled in this art. Without exception, they are all consistent with the Bingham references insofar as they fail to show circuitry such as the Examiner conjectures Tasdighi might show. Because they are consistent with the prior art incorporated in Tasdighi by reference, and are contrary to the Examiner's conjecture, these references buttress a conclusion that the Examiner's conjecture is contrary to the prior art, and to the practices of those skilled in the art.

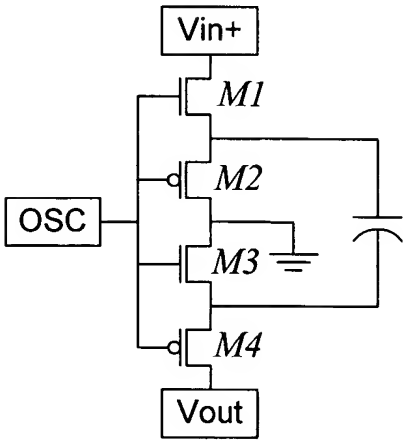
The Examiner failed to find an actual example of his conjectured circuitry. Absence of the conjectured circuitry from the modest quantity of prior art that is of record does not prove it cannot be found. However, because this is a crowded field with numerous patent references available, the Examiner's failure to locate an actual example of his conjectured coupling details is itself further significant evidence that such details do not exist in the prior art.

VII.A.1.e Tasdighi's Charge Pump Technically Needs Plural Clock Phases

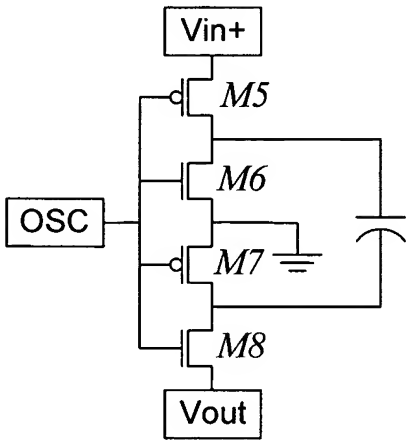
As has been noted above, the prior art of record, particularly that incorporated by reference in Tasdighi itself, invariably employs plural clock phases (or active coupling via an inverter, to the same effect). However, the prior art of record is only a modest part of the prior art to be found in this crowded field. Accordingly, a technical description is set forth below that illustrates how coupling such as that conjectured by the Examiner, in the absence of literal description, leads to inefficient and undesirable current spikes. This information is not essential to reverse the Examiner's rejection, but it explains why the circuit assumed by the Examiner would not be used by a skilled person. It therefore buttresses a conclusion that such a circuit will not be found in the prior art, and would not be taught or suggested by the prior art.

Tasdighi does not disclose the details illustrated below, but these two examples are presented *arguendo*, as the only ways to construct a circuit that is consistent with the Examiner's assumptions. By explicitly showing the circuit conjectured by the Examiner, its technical flaws become apparent:

Example 1



Example 2



In *Example 1*, M1 and M2 correspond to MOSFETs 26 and 27 of SW1, while M3 and M4 correspond to MOSFETs of SW2. Note that Vout is approximately -(Vin+), and that the capacitor is also charged to approximately Vin+. The problem with the circuit as conjectured by the Examiner is as follows: "Conventional CMOS inverters," such as the combination of M1+M2, function properly when they are coupled between unipolar supply rails (*e.g.*, coupled between a single supply consisting of "Vin+" and "ground"). However, when coupled between split supplies ("Vin+" to ground, and "Vout" to ground as in Tasdighi), they create current spikes.

To charge the capacitor, M1 and M3 must be turned on, and M2 and M4 must be turned off. This will require a "high" oscillator output (the voltage is a function of FET design, but obviously may not be lower than a "low" oscillator output, and must turn on both M1 and M3). To discharge, the opposite MOSFETs must be on, requiring a "low" oscillator output. As the clock voltage drops, it is critical that M3 turn "off" before M2 turns "on," because if both are turned "on" concurrently the capacitor is "shorted," causing at least a counterproductive current spike that will discharge the capacitor before it is coupled across the output supply. However, because M3 is necessarily at some potential below ground, while M2 is at some potential above ground, there is no threshold voltage

between Vin+ and Vout that meets the requirement. As the clock voltage falls from a "high" voltage that is sufficient to turn on M1, to a "low" voltage that is sufficient to turn on M4, M2 and M3 will necessarily be biased "on" concurrently.

Tasdighi describes "high" and "low" outputs in a simplified manner. The simplified description of the outputs, again due to a lack of detail, obscures the fact that the oscillator output cannot instantaneously transition between low and high. Consider a "high" voltage of 1/2 (Vin+), and a "low" voltage of 1/2 (Vout). Because the switching devices are "standard inverters," the thresholds of the NMOS transistors will be identical, and the thresholds of the PMOS transistors will also be identical. Accordingly, M3 will remain turned "on" until the clock voltage drops to (ground - 1/2 Vin+), (*i.e.*, negative Vin+/2). However, M2 will be turned "on" as soon as the clock voltage drops below (ground - 1/2 Vout), (*i.e.*, positive Vout/2). Thus, for the entire duration of the time that the clock falls from a positive value of Vout/2 to a negative value of Vin+/2, M2 and M3 are both "on," thus placing a direct short across the capacitor, which was charged to Vin+ volts. Large currents will flow that discharge the capacitor to itself, rather than to the output. This is a wholly unacceptable design due to the large resultant current spikes.

A comparable result follows in *Example 2*, except that the "outside" FETs M5 and M8 conduct concurrently, rather than the "inside" FETs M2 and M3 as in *Example 1*. M6 must be able to be turned on with less than Vin+ volts, while M7 must be able to be turned off with a voltage that is less negative than Vout (*i.e.*, smaller than -Vin+ volts). Consequently, when the clock signal is near ground, both M5 and M8 are fully turned on. When M5 and M8 are both conducting, the transfer capacitor is coupled directly across both positive and negative (output) supplies. This is similarly unacceptable, causing high and inefficient current spikes.

Thus, any circuit that conforms to Tasdighi, and is also consistent with the Examiner's conjectured passively coupled connections, is technically undesirable, rendering the charge pump unsuitable for its intended purpose. As such, a skilled person would <u>not</u> interpret Tasdighi in accordance with the conjecture of the Examiner, but would realize that something more is needed for the circuit to work properly. Such skilled person would likely conclude that an active circuit, such as

taught by Bingham '774 and incorporated by reference in Tasdighi, would be needed to properly control the coupling of a clock to the TCCSs so as to operate suitably.

The undesirability of the Examiner's conjecture is consistent with the observed fact that the prior art of record, in "control only" charge pump architectures such as Tasdighi's, all employ a plural phase clock and/or active coupling. With all due respect, the Examiner should not put himself forth as qualified to design a suitable circuit that is missing from his chosen cited reference, Tasdighi, particularly when his design is contrary to all of the prior art of record, and particularly when Tasdighi contains a suitable design that is incorporated by reference.

The technical explanation set forth above buttresses the conclusion, drawn above from the prior art that is of record, that prior art charge pumps comparable to that of Tasdighi would not be coupled passively to a single-phase clock, in the manner that is required by Claim 18. Such conclusion would preclude even a finding of obviousness of Claim 18 over Tasdighi, as is remarked upon below in regard to obviousness rejections of Claim 18 issued by the Examiner.

VII.A.1.f Other Doctrines for Asserting Missing Descriptive Material are Also Unavailing

The Examiner has not provided any actual doctrine under which the missing descriptive matter might properly be attributed to Tasdighi in spite of its clear literal absence. However, despite the failure of the Examiner's proffered rationales to support his conclusions, the Appellants have endeavored to address any alternative argument that could reasonably be set forth to justify the Examiner's conclusions.

Alternative doctrines for considering apparently missing descriptive matter to be present in a cited reference include taking "official notice" and citing to "common knowledge." All such doctrines are construed very narrowly, lest the exception swallow the rule requiring substantial evidence to support conclusions. *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Zurko III) (Fed. Cir. 2001)[3] ("[D]eficiencies of the cited references cannot be remedied by the [reviewing entity's] general conclusions about what is "basic knowledge" or "common sense" to one of ordinary skill in the art." Most certainly, appeal to such doctrines would be wholly improper when, as here, the asserted "facts" (*i.e.*, those asserted to be present in a reference despite their literal omission therefrom) are not merely unsupported by the prior art of record, but are, in fact, contrary to the

relevant disclosure in such prior art. For much the same reasons, the missing descriptive matter is not inherently present in Tasdighi.

Inherent disclosure is interpreted very narrowly: "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." (emphasis added) *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991)[4]. The record of this application includes no such evidence; to the contrary, the evidence of record in this application is contrary to the missing descriptive matter the Examiner would attribute to Tasdighi.

Conclusion: All of the reasons and facts set forth above support a conclusion that Tasdighi fails to disclose, teach or fairly suggest any of the three distinct elements defined by the underlined elements of Claim 18 (the missing descriptive matter). Even less, then, does Tasdighi teach the combination of all three elements, cooperating as required by the claim. Tasdighi thus fails to anticipate Claim 18, because all elements must be present and cooperating as claimed to anticipate the claim. *See, e.g., In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)[5] "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." (cites) "These elements must be arranged as in the claim under review, ..." *In re Bond, id.* at 832. It is respectfully submitted that the foregoing remarks, facts and law require a conclusion that the Examiner's rejection of the Appellants' Claim 18 under 35 USC 102, as anticipated by Tasdighi, is improper. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

VII.B. Rejections Under 35 USC § 103

VII.B.1 Rejections under 35 USC 103(a) over Tasdighi in view of Yamauchi

Claims 1-4, 10, 12, 14, 16, 19-20, 28-33, 36, 40, 43-44, 48-51, 53-54 and 57-58 stand rejected under 35 USC 103(a) as obvious over Tasdighi in view of Yamauchi. This ground for rejection is respectfully traversed as improper for lacking sufficient evidence to support even a *prima facie* case of obviousness of any of the rejected claims. Rejected dependent claims also include

further limitations not taught by the cited references, and thus do not rely for patentability on the claim(s) from which they depend.

VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi

A combination of Tasdighi in view of Yamauchi, considered as it must be in view of other prior art (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)[6], "*W.L.Gore*"), fails to render obvious the Appellants' Claim 1. *W.L.Gore* is one of the most frequently cited Federal Circuit cases, having been cited almost 600 times in judicial decisions, including over 100 times in subsequent Federal Circuit decisions, without eliciting a negative comment. The present facts (those regarding the rejection of Claim 1 over Tasdighi in view of Yamauchi) are extraordinarily closely analogous to those of *W.L.Gore*, and, as such, the reasoning of the court in *W.L.Gore* will be shown to clearly apply to the present facts to require a conclusion that Claim 1 is nonobvious over Tasdighi in view of Yamauchi. Indeed, the claims at issue in *W.L.Gore* were rejected over additional pairs of references, just as presently Claim 1 is also rejected over Tasdighi in view of Hara and Tasdighi in view of Ito, and the court's reasoning will be shown to require a conclusion that Claim 1 is nonobvious over each of the pairs of references.

To demonstrate the assertions set forth above, some relevant facts and legal conclusions of *W.L.Gore*, *id.* (endnote 6) are set forth below, together with a brief statement, in summary form, of the corresponding present facts, sufficient to show how the legal conclusions set forth in *W.L.Gore* apply to the present facts. Thereafter, said corresponding present facts are demonstrated in more detail, together with additional useful facts that help buttress a conclusion of nonobviousness for Claim 1 over all of the prior art references cited by the Examiner.

The various grounds of rejection of Claim 1 set forth by the Examiner are similar to those of *W.L.Gore*, *id.* (endnote 6) in that they are based on impermissible hindsight analysis. "In concluding that obviousness was established by the teachings in various pairs of references, the district court lost sight of the principle that there must have been something present in those teachings to suggest to one skilled in the art that the claimed invention before the court would have been obvious." *W.L.Gore*, *id.* (endnote 6) at 1551. In *W.L.Gore*, the district court was thus chastised because the cited prior art failed to teach an element, stretching of a particular polymer (unsintered, highly

crystalline PTFE), with a magnitude limitation on the rate of stretch (>100% per second in a claim at issue), and because, as the (Federal Circuit) court noted, "On the contrary, the art as a whole teaches the other way."

The present circumstances are analogous. There is no teaching in the cited prior art that the claimed invention, and particularly its element of a current-starved ring oscillator for a charge pump together with a magnitude limitation on the number of inverter sections (not more than three), is desirable. On the contrary, the art as a whole teaches the other way.

In *W.L.Gore*, a cited reference, Sumitomo, taught a basic element: stretching of unsintered PTFE without heating above the crystalline melting point. Sumitomo did not explicitly exclude stretching with the magnitude limit claimed by the claim at issue there. The court's assertion, above, that the cited art did not teach the claimed invention relied on the fact that Sumitomo failed to mention magnitude limits for the rate of stretching. In particular, "the court recognized that Sumitomo made no mention of rate of stretch." *W.L.Gore*, *id.* (endnote 6) at 1551. Presently, and analogously, a cited reference (Yamauchi) teaches a basic element: a current-starved ring oscillator for a charge pump. The corresponding magnitude limitation claimed in Claim 1 is to "not more than three" inverter sections. Like Sumitomo, Yamauchi does not teach the magnitude limitation, but also does not specifically exclude a three-inverter ring oscillator. Like Sumitomo, Yamauchi simply proposes no limitation at all on the possible number (here, of inverter sections in a ring oscillator, which must be an odd number to work, and which may need to be at least three to form a "ring").

The court in *W.L.Gore*, having concluded that the magnitude-limited element was not taught by the cited references, further concluded that the art as a whole taught away from the claimed stretching magnitude limitation. To reach this conclusion as to the claim at issue there, the court pointed to the fact that a secondary reference (Markwood), cited as teaching the claimed magnitude limitation, was teaching about a somewhat different "conventional" polymer, and by pointing further to art that suggested that unsintered PTFE does not respond to conventional processing. As the court summarized it: "The court's pairing of Sumitomo and Markwood disregarded, as above indicated, the undisputed evidence that the unsintered PTFE of Sumitomo does not respond to the conventional

plastics processing of Markwood and the art recognition of that fact." *W.L.Gore*, *id.* (endnote 6) at 1551 (emphasis added).

While the court in *W.L.Gore* had to look to several references to determine that the prior art as a whole taught away from the claimed invention, the present circumstances are much simpler. Hara, cited by the Examiner in another rejection of Claim 1, explicitly suggests a magnitude limitation for the number of inverters in a current-starved ring oscillator serving as a clock for a charge pump. That magnitude limitation is an odd number of five or more inverter stages (Hara, col. 5 lines 60-62). Thus, Hara teaches that any magnitude is acceptable, from among the possible numbers of inverters (*i.e.*, an odd number), except the number claimed by the Appellants! (This might be less surprising if the inventors had been aware of Hara at the time of invention, but they were not.)

As to the immediate ground of rejection of Claim 1 over Tasdighi in view of Yamauchi, moreover, the Examiner does not even point to a reference that suggests the claimed magnitude limitation, and thus this ground of rejection is far less compelling than that argued in *W.L.Gore*, *id.* (endnote 6). However, in another rejection the Examiner does point to a reference, Ito, for the magnitude limitation. While failing to actually suggest a magnitude limitation, Ito does include one illustration of a current-starved ring oscillator having only three stages.

Considering the rejection of Claim 1 over Tasdighi in view of Ito, the analogy to *W.L.Gore* remains extremely close. The magnitude-limit reference in *W.L.Gore*, Markwood, was inapplicable because other references showed that the stretch-rate teaching of Markwood were for conventional polymers, and were not applicable to unsintered PTFE. Ito, the only magnitude-limit reference of the three grounds of rejection applied to Claim 1, is general-purpose oscillator art, for use in voltage-controlled oscillators, and is inapplicable to charge pumps. Not only do the cited references lack any suggestion that three-stage ring oscillators are desirable for charge pumps, but two further facts point away from three-stage ring oscillators. First, of course, is the teaching of Hara that a charge pump clock current-starved ring oscillator should have five or more inverter stages, and that is clear. But moreover, there is other evidence suggesting that not all oscillators are suitable for use with charge pumps. In particular, a survey of the prior art of record shows that all charge pumps in the prior art

used rectangular or nearly rectangular clock waveforms; and it can be readily established that current-starved ring oscillator outputs become progressively (and substantially) less rectangular as the number of inverter stages declines. Thus, even though the Examiner tries by hindsight analysis to force the inappropriate Ito to fill the missing matrix element of the frame established by Claim 1, there is no suggestion that Ito is suitable for charge pumps, and substantial evidence that it is not.

The analysis above compares the present circumstances of the various rejections of Claim 1 to the facts in *W.L.Gore*, *id.* (endnote 6) in only summary form, and details of such circumstances are accordingly set forth below. The reasoning of *W.L.Gore* inescapably applies to said present circumstances, requiring that teaching in the prior art that is away from the claimed invention must be considered, at least when the cited references are devoid of any suggestion that the claimed invention is desirable. As in *W.L.Gore*, all of the references cited by the Examiner against Claim 1, including Tasdighi, Yamauchi, Hara and Ito, even taken all together, fail to suggest, either by example or textually, that a current-starved ring oscillator having not more than three inverter stages is desirable for a charge pump clock. Even more clearly than in *W.L.Gore*, the prior art includes evidence and teaching that is away from the claimed invention. As in *W.L.Gore*, then, Claim 1 is nonobvious over any pair of the cited references.

Factual Details and Additional Arguments for Nonobviousness of Claim 1 over Tasdighi in view of Yamauchi: Details of the points summarized above are set forth below, including, at the end of this subsection, a comparison of the facts of *W.L.Gore*, *id.* (endnote 6) to the present facts to support a conclusion that Claim 1 (and also Claims 40 and 43) is nonobvious over not only Tasdighi in view of Yamauchi, but also over Tasdighi in view of Hara and Tasdighi in view of Ito.

Claim 1, as presently pending, recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of <u>not more than three inverting driver sections</u> cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes

i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and

ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output;

Neither reference suggests the underlined limitation. On page 15 of the Final Rejection, the Examiner acknowledges: "However, the Tasdighi reference does not clearly show or disclose charge pump clock generating circuit 2 comprising a ring oscillator with no more than three inverting driver sections, or circuitry for limiting current at a driver section's output." Thus, the Examiner relies upon Yamauchi to disclose these elements of Claim 1 as set forth above. In so doing, the Examiner states that Figs 6 and 7 of Yamauchi show examples of a ring oscillator, "wherein each figure shows it can comprise only three inverter driver sections" (emphasis added).

However, Yamauchi fails to teach this narrow and explicit limitation. Yamauchi represents partially (Fig. 6) and fully (Fig. 7) current-starved ring oscillators, but teaches only that they should have an odd number of sections (which is required for oscillation). Yamauchi states (col. 10 lines 23-24) "Referring to Fig. 6, ring oscillator 39 is formed having an odd number of inverters connected in series." The same description of the number of inverter devices as simply "odd" is repeated elsewhere (*e.g.*, col. 10 lines 37-40 and col. 11 lines 48-51). There is no other teaching or suggestion of a limitation as to the magnitude of the number of inverter sections. Thus, it is clear that the description of Yamauchi is not intended to convey any narrower limitation on the number of inverters in a ring oscillator than that it be an odd number. An odd number of sections is, of course, required to reliably achieve oscillation under ordinary circumstances.

The illustrations of Yamauchi teach no more than the text noted above. Even though Figs. 6 and 7 of Yamauchi include schematic representations of only three driver sections, they do not suggest that an oscillator would include only three driver sections. This may seem surprising until the figures are carefully reviewed. Both figures include sequences of three dots between inverter driver sections. The three dots indicate that repetitive material has been omitted from the illustration. The implication is that additional driver sections are ordinarily included, but have been omitted from the drawing to avoid obscuring detail. The figures simply illustrate a ring oscillator as

described by the text: having an odd number of inverters connected in series. A single inverter is not "inverters connected in series," so the smallest number is three. Hence, the illustrations represent three or more inverter stages. Because a ring oscillator must have an odd number of inverter stages to work correctly, that is no limitation on the magnitude of the number of inverter stages. Yamauchi thus in no way suggests that the magnitude of the number of inverters should be limited at all, let alone that it should be limited to no more than three sections. For the reasons set forth above, in contrast to the Examiner's assertions, the abbreviated illustration shown in Figs 6 and 7 of Yamauchi do not teach or suggest that the ring oscillator is limited to comprising not more than three inverting driver sections as set forth in Claim 1.

Ring Oscillator Length and Resultant Waveforms: Hara's teaching away from "no more than three" inverter stages in a current-starved ring oscillator for a charge pump clock is quite clear from Hara, col. 5 lines 60-62. However, the prior art teaches away from this limitation also by the facts that rectangular waveforms are preferred for charge pumps, and that small numbers of inverter stages in a current-starved ring oscillator cause the output waveform to be progressively, and substantially, non-rectangular.

A current-starved ring oscillator of not more than three sections helps solve the Appellants' problem of avoiding noise generation for a technical reason. The technical reason is that a current-starved ring oscillator having not more than three sections has a relatively rounded waveform with relatively slow rise and fall times. That reason is also precisely why such oscillators have been avoided in prior art charge pump designs, because conventional charge pump practice employs clocks having edges that are as sharp as is conveniently possible. Conventionally, fast rise and fall times reduce uncertainties in timing and overlap, ensuring (in conjunction with proper timing control) that switches are turned on for as long as possible while preventing concurrent conduction of switches that are disposed in series across a supply or a transfer capacitor (see, *e.g.*, US Patent 5126590 to Chern, col. 1 lines 19-27; also, fast-edged clocks are so ingrained in charge pump design that, for example, US Patent 6518829 to Butler teaches square-edged clocks despite being directed to solving the problem of lowering noise, see the abstract and Figs. 3-6). While all voltage transitions take finite time to occur, the prior art consistently teaches generating relatively square charge pump clock waveforms.

Thus, from the conventional charge pump standpoint, the problem with using only three stages in a current-starved ring oscillator is that they do not produce very square output waveforms. Increasing the number of inverter stages in a current-starved ring oscillator decreases the proportion of the output period that is required for each transition between low and high levels. Increasing the number of inverter stages from three to even five substantially increases the "squareness" of the waveform.

A survey of the prior art of record that is set forth below (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*), establishes that each and every prior art reference that is of record in this Appeal, and which includes sufficient information to determine clock waveform, teaches the use of square, or nearly square, charge pump clock waveforms. Clearly, conventional charge pump designers greatly prefer clocks that have relatively fast transitions, *i.e.*, that are relatively square. 3-section current-starved ring oscillators do not satisfy this preference. Rather, the transition time in their waveforms is a much greater proportion of the period in a three-stage current-starved ring oscillator than in an otherwise similar design having more stages, and the shape of the resultant waveform is more rounded, even significantly sine-like. This incompatibility with technically preferable waveforms for charge pump clocks explains why a 3-section current-starved ring oscillator for a charge pump has not been found in the prior art of record (despite the obvious advantages of parts reduction), and also suggests that it will not be found in any prior art.

Analysis Without W.L.Gore It is not necessary to follow *W.L.Gore*, *id.* (endnote 6) to establish that Tasdighi in view of Yamauchi fails to render Claim 1 obvious. First, neither of the cited references teaches or fairly suggests the limitation to "not more than three inverting driver sections" underlined below. This failure of disclosure is despite the fact that ring oscillators are common, and current-starved ring oscillators not uncommon, in the charge pump prior art of record. Second, an example of a current-starved ring oscillator for a charge pump having three (or less) stages is absent from all of the prior art of record, and presumably from all of the prior art searched by the Examiner. Third, the absence of such example immediately implies that those of skill in the art avoid using three (or less) stage current-starved ring oscillators with charge pumps, both because charge pumps constitute a crowded field having hundreds of patent references, and because the specified example, having the obvious advantages of containing the fewest components of any such

ring oscillator, would be expected to be the most common example. Fourth, the specified example tends to cause a waveform that is less rectangular than any clock waveform in the prior art of record. All four of these reasons imply that the specified example is contrary to the practice of those skilled in the art, and would thus fail to support *prima facie* obviousness of the specified limitations, but this implication is firmly buttressed by the presence, in prior art cited in other rejections, of explicit teaching away from the specified limitations.

It has long been established that to establish *prima facie* obviousness, all of the claim limitations must be taught or suggested by the prior art. "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)[7]. Yamauchi and Tasdighi both fail to suggest the limitation to "not more than three inverter driving sections" that is recited in Claim 1. That is a sufficient reason to conclude that the combination of these two references fails to support *prima facie* obviousness of Claim 1. However, further reasons to conclude that the combination of cited references fails to support *prima facie* obviousness follow.

In view of the obvious advantages, the absence of an example of this feature in the extensive prior art in this crowded field buttresses its nonobviousness. Current-starved ring oscillators are known to be used with charge pumps. However, it is respectfully submitted that the prior art, including the prior art of record and that which has been searched by the Examiner, does not teach, in a charge pump, using a current-starved ring oscillator that has no more than three sections. The Appellants' representative is unable to find such after substantial review of the references, and certainly the Examiner has not indicated where such material might be found.

On page 16 of the Final Rejection, the Examiner states: "The use of a ring oscillator with only three driver sections will require fewer elements, take up less area, and consume less overall current, than a ring oscillator having a higher, odd number of driver sections."

It is axiomatic that good designers endeavor not to use any more circuitry than necessary to accomplish their purpose. The evidence shows that current-starved ring oscillators are frequently used with charge pumps; hence, in view of the quite obvious advantages of using fewer stages for ring oscillators, one would certainly expect the smallest simple design (three inverter stages) to be

the most commonly implemented. The fact that there is no extant example of such a ring oscillator at all in the prior art of record, and, so far as is known, none elsewhere in the prior art, is therefore quite surprising. The absence of an example of the claimed feature, in this field crowded with examples of ring oscillators, strongly implies that there is a compelling reason, known to those of skill in the charge pump art, to avoid use of a current-starved ring oscillator comprising not more than three inverting driver sections, rendering such a design nonobvious over the prior art.

Hara, the only prior art that suggests a magnitude restriction on the number of inverter stages in a current-starved ring oscillator, teaches directly away from the claimed feature. Of all the prior art of record, Hara is the charge pump reference that deals most explicitly with current-starved ring oscillators. Moreover, the clock waveform illustrated in Hara is one of only two that deviate from essentially perfect squareness (Chern has one waveform with a 9% larger transition/period ratio), indicating that Hara has more tolerance for a lack of squareness than other prior art. Furthermore, Hara is also the only prior art reference that makes any statement whatsoever regarding the magnitude range of the number of ring oscillator inverter stages for a charge pump. In view of (1) the obvious advantages of use of fewer inverter stages as pointed out by the Examiner, (2) the relative tolerance to nonideal clock waveforms of Hara, and (3) the detailed examination of current-starved ring oscillators in Hara, it is reasonably to be expected that Hara would teach that a current-starved ring oscillator having a small number of inverter sections (*e.g.*, three) is the most desirable, or is, at least, acceptable. The surprising fact is exactly to the contrary: Hara explicitly suggests that at least five sections should be employed in a current-starved ring oscillator (*see* Hara, col. 5 lines 60-62, Figs. 1 and 4-6). Hara thereby recommends against the very size of ring oscillator that is required by (*e.g.*) Claim 1. (Note that three is the preferred number of inverters in the Appellants' design, as developed prior to awareness of Hara.)

For all of the reasons set forth above, Claim 1 is nonobvious over Tasdighi in view of Yamauchi. Moreover, in view of the analysis of *W.L.Gore*, *id.* (endnote 6) that is set forth above with supporting facts, it is respectfully submitted that Claim 1 is nonobvious over all three pairs of cited references, and indeed over Tasdighi, Yamauchi, and Hara taken all together (Ito would not be followed for charge pump oscillators). Finally, because Claim 43 has similar limitations as Claim 1,

and further by virtue of dependency, the panel is respectfully requested to reverse the Examiner as to all grounds of rejection of Claims 1 and 43 and all those depending therefrom.

VII.B.1.b Rejection of Claims 2-4 and 10 over Tasdighi in view of Yamauchi

Claim 2: Claim 2, as presently pending, recites: "The apparatus of Claim 1, wherein the plurality of transfer capacitor coupling switches are under control of the particular charge pump clock output." This refers to clause (b) of Claim 1, which recites: "a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output," and the particular charge pump clock output of clause (c) of Claim 1. It is respectfully submitted that Tasdighi fails to teach or fairly suggest the limitation recited in Claim 2. As noted above in subsection *VII.A.1.b Literal Disclosure of Tasdighi versus Disclosure Attributed by the Examiner*, Tasdighi provides only an arrow pointing between oscillator and switching blocks to suggest coupling. The arrow contains no specific electrical information, and cannot support the Examiner's conjecture as to details of the coupling. Yamauchi also discloses no charge pump switching or clock coupling details. Accordingly, the combination of Tasdighi and Yamauchi fail to disclose all of the limitations of Claim 2. Thus, Claim 2 is nonobvious over Tasdighi in view of Yamauchi by virtue of depending from Claim 1, and additionally nonobvious for this additional reason. Because Tasdighi in combination with Yamauchi fails to establish even *prima facie* obviousness of Claim 2, the panel is respectfully requested to reverse the Examiner's rejection of Claim 2 over Tasdighi in view of Yamauchi.

Claim 3: Claim 3 is nonobvious for all of the reasons applicable to Claim 2, and is moreover further nonobvious over Tasdighi in view of Yamauchi for the reasons set forth below with respect to Claim 4.

Claim 4: Claim 4 depends from Claim 1. Both Claims 3 and 4 include a further requirement that the clock signal be coupled to the switches "without increasing a rate of voltage rise or fall of the signal." Both Tasdighi and Yamauchi fail to disclose this implementation requirement, disclosing only an arrow (FIG. 2 of Tasdighi, FIG. 5 of Yamauchi) to indicate coupling of the clock to the charge pump switches. Because the arrow is not an electrical symbol, and conveys no detail whatsoever about such coupling, the combination of references fails to disclose the further limitation

recited in Claims 3 and 4. Accordingly, this combination of references does not support *prima facie* obviousness of either of Claims 3 and 4 for at least this additional reason.

A further consideration renders Claims 3 and 4 even more contrary to the prior art in view of the limitation in Claim 1 to a clock which, as noted, tends to produce a relatively slow clock waveform that is far from square. The prior art of record (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*) indicates that sharp edged clocks having square or nearly square waveforms are used exclusively in the prior art. As such, even if prior art were found that disclosed a three-stage current-starved ring oscillator for use with charge pumps, it is highly likely that such prior art would include a conditioning circuit to "square up," or increase the voltage rise and/or fall times of the clock signal. As such, Claims 3 and 4 are not only undisclosed by both Tasdighi and Yamauchi, but are furthermore contrary to the expected practice of charge pump designers.

For all of the reasons set forth in this subsection, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 3 and 4.

Claim 10: In addition to the limitations of Claim 1, Claim 10 further requires "coupling substantial charge into the transfer capacitor via the charge pump clock output." The same lack of coupling detail in Tasdighi described above (*see, e.g.*, subsection *VII.A.1.b Literal Disclosure of Tasdighi versus Disclosure Attributed by the Examiner*) precludes a conclusion that Tasdighi discloses this particular feature. Yamauchi, also as noted above, has no coupling details whatsoever. Consequently, the combination of Tasdighi and Yamauchi does not disclose all of the limitations of Claim 10 for at least this reason. As such, this combination of references fails to establish *prima facie* obviousness of Claim 10.

Misinterpretation of the word "via" The Examiner supports his rejection of Claim 10 over Tasdighi and Yamauchi by stating (page 16 lines 15-18): "Since transfer capacitor C1 will be periodically coupled between voltage source Vin and Gnd in response to the charge pump clock output in order to charge, a substantial charge will be coupled into transfer capacitor C1 during those periods, rendering claim 10 obvious." The Examiner has apparently incorrectly construed the language of Claim 10, which recites (underlining added for emphasis): "coupling substantial charge into the transfer capacitor via the charge pump clock output." The language plainly means that the

substantial charge passes through the clock output itself, and not, as the Examiner would have it, that charge is coupled into the transfer capacitor under control of the clock output. The plain meaning of the term "via" is "by way of," not "under control of." This appears to be the Examiner's mistake, because otherwise his rejection is illogical in view of the insulating nature of CMOS gates. Even assuming *arguendo* that the charge pump clock is directly coupled to the gates of the CMOS FETs in SW1 and SW2 (as asserted by the Examiner), such coupling would clearly not transfer substantial current into C1 "via the charge pump clock output", as set forth in Claim 10. The only current that would be coupled from the clock into C1 in such a charge pump would be tiny amounts due to parasitic gate capacitance of the FETs. The modifier "substantial" is included in Claim 10 precisely to preclude such incidental parasitic charge transfer from "reading on" the claimed limitation.

Claim 10 is nonobvious over Tasdighi in view of Yamauchi by virtue of depending from Claim 1, and additionally for the reasons set forth above. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 10.

VII.B.1.c Rejection of Independent Claim 43 over Tasdighi in view of Yamauchi

Claim 43 is a method claim that corresponds generally to Claim 1. In particular, Claim 43 requires (underlining added for emphasis): "b) limiting source current provided to each inverting driver output node of a current-starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator." As such, all of the arguments set forth above in subsection *VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi* are directly applicable to support a conclusion that Claim 43 is also nonobvious over this combination of references. Tasdighi does not disclose any oscillator details. Yamauchi does not suggest any particular magnitude range for the number of inverter stages, requiring only that it be an odd number (necessary for oscillation). Moreover, the evidence of record in this application supports a conclusion that one of skill in the art would not use a current-starved ring oscillator of only three inverter stages to generate a charge pump clock, despite its obvious advantages of reduced power consumption, reduced chip area, and so on.

Claim 43 is nonobvious over the cited references for all of the reasons set forth in subsection *VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi*, and the following remarks buttress the nonobviousness of Claim 1, as well as of Claim 43, over the cited references.

Appellants' realization that a fast clock was a problem for charge pumps requiring reduction of noise generation led the Appellants to reject the conventional teaching of those skilled in charge pumps. The Appellants realized that a slow clock, though eschewed by the conventional practice of those skilled in the charge pump arts, could help solve the problems associated with excessive electrical noise generation. A current-starved ring oscillator, by having less inverter stages than has previously been taught for charge pumps, can generate a slow clock and thereby alleviate the generation of noise in the charge pump incorporating it. That this particular range (of inverter sections) would solve, rather than create problems, is clearly unexpected in view of the absence in the prior art of any actual example of such a design.

The prior art, even when addressing the problem of noise generation, teaches the use of fast-transitioning clocks. Fast-transmitting clocks are also taught by those endeavoring to reduce charge pump noise (see, *e.g.*, US Patent 5126590 to Chern, as remarked upon above with respect to the rejection of Claim 1 over Tasdighi in view of Yamauchi).

That the Appellants contravened the prior art practice of those skilled in the art is supported by the following summary of facts. First, the prior art provides no explicit suggestion of using only three inverter stages in a charge pump clock, despite the frequent appearance of similar current-starved oscillators having a larger numbers of inverters, and despite the apparent economies of using less stages. Second, Hara teaches directly away from use of 3 or less stages (*see* portion *Further analysis buttressing a conclusion that three-stage current starved ring oscillators are contrary to charge pump prior art:*, which is located in sub-subsection **Claim 40:** of subsection *VII. B.1.i Rejection of Claims 29-33, 36 and 40 over Tasdighi in view of Yamauchi*, which description is incorporated here by reference for its analysis of the teaching, by Hara, that current-starved ring oscillators for charge pump clocks should have five or more stages). Third, a current-starved ring oscillator of few sections generates a waveform that is far from square because a high percentage of the oscillation period is necessarily occupied by transition (*see* description regarding **Claim 40** as

noted above), and unsquare clock waveforms are contrary to the prior art of record (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). Particularly where the cited prior art is silent as to a claimed magnitude range, as presently, other prior art teaching away from the magnitude range must be considered, and will render the claimed magnitude range nonobvious. (see, *W.L.Gore, id.*, endnote 6.) Accordingly, for these reasons, and those set forth above, Claim 43 is clearly nonobvious over the combination of Tasdighi and Yamauchi.

In view of the remarks set forth above in this section, as well as those set forth above in subsection *VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi*, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 43, and also as to Claim 1.

VII.B.1.d Rejection of Claims 44 and 48 over Tasdighi in view of Yamauchi

Claims 44 and 48 include all of the limitations of Claim 43, and are accordingly nonobvious over Tasdighi in view of Yamauchi for all of the reasons set forth above. Claim 44 is permitted to stand or fall with Claim 43.

Claim 48 recites in part (underlining added for emphasis): "further comprising coupling the first charge pump output as a signal to a control node of the discharging switch circuit via a network that is not configured to increase rates of voltage change of the signal." This element is similar to those recited in Claims 3 and 4. As such, the remarks set forth above in subsection *VII.B.1.b Rejection of Claims 2-4 and 10 over Tasdighi in view of Yamauchi* with respect to Claims 3 and 4 is applicable, properly supporting a conclusion that Claim 48 is further nonobvious over Tasdighi and Yamauchi in view of this claim element. Those remarks are accordingly incorporated here by reference.

Tasdighi and Yamauchi both fail to teach, disclose or fairly suggest the recited element of Claim 48, especially as underlined above. In respect of coupling the clock to charge pump switches, each reference discloses only a simple arrow, which conveys no electrical significance, pointing from one block to another. In view of the absence of at least this limitation of Claim 48, the combination of Tasdighi and Yamauchi fail to sustain *prima facie* obviousness of Claim 48. Claim 48 is thus properly allowable over these two cited references irrespective of the allowability of Claim

43, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 48.

VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record

The prior art of record indicates that those of skill in the charge pump art had invariably used clocks having waveforms that were rectangular or nearly rectangular in shape. The prior art references of record that illustrate clock waveforms are set forth below, together with a description of the clock waveform that they illustrate. (Numbers are as assigned in the Evidence Appendix):

Reference:	Clock Waveform
2. U.S. Patent No. 6,411,531 (Nork, et al.)	Rectangular (Figs. 3B, 6B, 8B)
3. U.S. Patent No. 6,518,829 (Butler)	Rectangular (Figs. 4, 5, 6)
9. U.S. Patent No. 5,446,418 (Hara, et al.)	Nearly rectangular (Fig. 16)
13. U.S. Patent No. 4,621,315 (Vaughn, et al.)	Rectangular (Figs. 2)
15. U.S. Patent No. 4,703,196 (Arakawa)	Rectangular (Fig. 4)
17. U.S. Patent No. 4,769,784 (Doluca, et al.)	Rectangular (Fig.4)
21. U.S. Patent No. 5,068,626 (Takagi, et al.)	Rectangular (Figs. 3, 5A, 5B)
23. U.S. Patent No. 5,111,375 (Marshall)	Rectangular (Fig. 6)
24. U.S. Patent No. 5,126,590 (Chern).	Nearly rectangular (Fig. 3)
26. U.S. Patent No. 6,130,572 (Ghilardelli, et al.)	Rectangular (Figs. 2, 5)
27. U.S. Patent No.6,816,000 (Miyamitsu)	Rectangular (Figs. 3, 4, 7, 11)
28. U.S. Patent No. 6,816,001 (Khouri, et al.)	Rectangular (Fig. 7)
29. U.S. Patent No. 6,825,730 (Sun)	Rectangular (Fig. 3)
30. U.S. Patent No.6,831,847 (Perry)	Rectangular (Figs. 6a, 6b, applied 6c, 6d)

27 illustrations in these 14 references illustrate clock waveforms, of which 25 are essentially perfectly rectangular. Two figures, one each in Hara and Chern, show nearly rectangular, slightly trapezoidal waveforms. This evidence supports a conclusion that persons skilled in the charge pump arts traditionally rely upon fast clocks having square or nearly square output waveforms.

The prior art of record is believed to contain not the slightest suggestion that highly unsquare or sine-like waveforms might be even marginally acceptable. Moreover, Hara teaches that current-

starved ring oscillators should not have less than the five inverter stages that produce the waveform illustrated in Fig. 16. Because fewer stages would make the waveform less square, and because no prior art waveform is significantly less square than that of Fig. 16 of Hara, the clear implication is that a less-square waveform is considered unacceptable.

VII.B.1.f Rejection of Independent Claim 12 over Tasdighi in view of Yamauchi

A sine-like charge pump clock waveform is contrary to the goals and practices of prior art charge pumps. As may be seen from the immediately preceding subsection, prior art clock waveforms are as close to perfectly rectangular as can conveniently be achieved, so that transfer capacitor currents can remain high for as long as possible, yet without causing damaging "shorts" across the terminals of a transfer capacitor or a supply. The steep-edged clocks of the prior art, however, contain large energies at higher frequencies (harmonics of the fundamental clock frequency). Such high frequency signal components readily couple throughout the integrated circuit. By contrast, mathematics defines that more a signal approximates a sine wave, the smaller is the harmonic content of the signal. Not only is less noise generated by such a clock, it will also tend to cause the charge pump switching circuits to switch more slowly, thus reducing the di/dt of current conducted through the transfer capacitor. Paragraph 50 of the Appellants' specification includes a description of the desire for low switching rates (dv/dt and di/dt), culminating in a clock waveform having a significantly sine-like shape.

Claim 12 recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to
>
> i) circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and
>
> ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

To support the rejection of Claim 12 over Tasdighi in view of Yamauchi, the Examiner asserts in regard to Yamauchi's Fig. 7 (page 17 beginning of line 4 of the Final Rejection, underlining added for emphasis): "The periodic switching of 43 and 45 will effectively provide a

CLK waveform that can be considered substantially sine-like." The Appellants' representative respectfully submits that this ground for rejection is a further example of a rejection based upon pure conjecture by the Examiner of features that are not only not in evidence, but that are contrary to all of the evidence of record. Despite the Examiner's assertion to the contrary, the CLK waveform of Yamauchi cannot properly be considered substantially sine-like.

The Federal Circuit is sometimes brusquely dismissive of the conjecture and hindsight analysis of a district court, as demonstrated by this acerbic passage in an opinion: "That one *could* invent such a cable tie is unquestioned. Caveney *did*. The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made." *Panduit Corporation V. Dennison Manufacturing Co.*, 774 F.2d 1082,1092, 227 U.S.P.Q. 337, 347 (Fed Circuit, 1985)[8](emphasis in original). The court's apparent pique appears to reflect growing impatience over the district court's extensive use of conjecture and hindsight analysis to justify holding a claim obvious over the prior art. The quote above follows a summary of errors by the district court, of which a portion is set forth below:

> *(b) The Errors*
>
> En route to its decision on obviousness, the district court was led to these errors:
>
> (1) It employed the benefit of hindsight.
>
> (2) It misinterpreted the claimed inventions.
>
> (3) It misevaluated the prior art.

Panduit, id., endnote 8, at 1091. It is respectfully submitted that the Examiner is making each and every one of these errors in the present case. As to (1) hindsight, it is plainly demonstrated above in subsection *VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi* that the Examiner attributed disclosure to Tasdighi that was not literally present there, that was contrary to descriptive material incorporated in Tasdighi by reference, contrary to all of the prior art of record, and contrary to proper design practice, all so as to assert that Tasdighi "disclosed" the invention claimed in Claim 18. The elements, not being available in any prior art of record, could only have been deduced by the Examiner through hindsight analysis, relying on the claim itself as a template. The same facts

support a conclusion that the Examiner (3) misinterpreted the prior art, Tasdighi. But the issue that is most relevant to Claim 12 is that the Examiner has (2) misinterpreted the claimed invention, as is demonstrated by the remarks in the following two paragraphs.

It is a basic tenet of claim construction that a limitation is given its plain meaning, *i.e.*, its ordinary and customary meaning, unless the applicant or patentee has made a contrary meaning clear in the specification. "In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art." *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298, 67 USPQ2d 1132, 1136 (Fed. Cir. 2003)[9]. The usual and customary meaning of a term may be evidenced by a variety of sources, such as dictionaries (*Tex. Digital Sys., Inc., v. Telegenix, Inc.*, 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1818 (Fed. Cir. 2002)[10]).

In the present case, it should not be necessary to explain the plain, usual and customary meaning of a "sine" waveform, because the mathematical definition is so fundamental to the education of electrical engineers. Certainly, one of skill in the art of charge pumps would be expected to be an electrical engineer. Nonetheless, a dictionary definition is provided: a "sine wave" is defined as "a periodic oscillation, as a sound wave, having the same geometric representation as a sine function." In the same dictionary, a "sine curve" is defined as "a curve described by the equation $y = \sin x$, the ordinate being equal to the sine of the abscissa." ("Webster's Encyclopedic Unabridged Dictionary of the English Language," pub. Gramercy Books, copyright 1989 by dilithium Press, Ltd.). It is respectfully submitted that the Examiner's proffered definition entirely fails to comport with the central "sine function" aspect of the dictionary definition. Thus, the Examiner misinterpreted the plain meaning of the claimed invention, as noted above.

The Appellants intend the plain, usual and customary meaning of the words of the limitation, and have done nothing to cause any other definition to be imposed. The Examiner complains that the limitation "substantially sine-like" is not explained sufficiently for his understanding. The Examiner stated: "Therefore, clarification is requested that clearly explains what this "sine-like" limitation actually means. For example, the original disclosure only mentions the output voltage "may oscillate substantially rail-to-rail ... and may have a significantly sine-like shape" on the last

lines of paragraph 050 (see page 12)." (Final Rejection, beginning last line of page 7, emphasis in original). The Examiner's lack of understanding of these common words is, with all due respect, astonishing for one who is supposed to have some knowledge in electronics.

The Appellants provided no further definition, believing that defining "sine" was not only unnecessary, but indeed would be insulting to those of skill in the electrical engineering arts concerned with charge pumps. In any event, the Examiner's statement makes clear that the Appellants did not provide explanation or alternative definitions that might convey "an express intent" to avoid the plain meaning of the term "sine," or the corollary limitation "sine-like." Therefore, the Appellants are entitled to have the terms of the limitation construed according to its widely understood plain, usual and customary meaning, precisely as they intended (*Brookhill-Wilk 1*, *id.*, endnote 9).

It is respectfully submitted that the prior art of record supports a conclusion that the clock waveforms employed by those of skill in the art were rectangular, or nearly rectangular, and that there is not the least suggestion of a clock waveform that is "substantially sine-like," nor of any waveform that is comparable (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). Expert testimony is not readily entered during this appeal, but the following statement is nonetheless respectfully submitted as being clearly apparent to those of even modest familiarity with electrical waveforms: a rectangular, or nearly rectangular waveform, as found in the prior art, is not "substantially sine-like," but to the contrary is far from a curve following "the sine function," and thus the limitation at issue cannot fairly be considered disclosed anywhere in the prior art of record, let alone in one of the cited references as required to support this ground of rejection. Further demonstration of the failure of the cited references to remotely suggest the "substantially sine-like" limitation is set forth below.

Yamauchi consistently describes the signal "CLK" as "(pulse voltage)" (col. 9 line 66, col. 10 lines 1 and 13). To those skilled in the art, "pulse voltage" suggests very sharp rise and fall times; in any event, it in no way implies or suggests a sine-like shape. Furthermore, every reference of record that describes or illustrates a clock waveform shows a waveform that is square, or nearly square. Fig. 7 itself gives no suggestion of the shape of the waveform of the signal CLK.

Tasdighi refers to the clock waveform as a "train of pulses" (col. 3 lines 16-17). This language is consistent with a description of square or rectangular waveforms, and is inconsistent with a description of a sine or sine-like waveform. Thus, the evidence in both cited references is that the clock waveforms should "be considered" to be pulses, or a train of pulses. This is entirely consonant with the other prior art of record, which illustrates no clock waveforms that are not rectangular or nearly rectangular ((*See* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). However, it is directly contrary to the assertion by the Examiner that such oscillating pulse voltage "can be considered substantially sine-like." Thus, the Examiner's assertion is entirely unsupported by the evidence in the cited references Tasdighi and Yamauchi, and is also contrary to all of the relevant prior art that is of record in this application.

Based on the ordinary meaning of the term "substantially sine-like," which would be readily understood by those of even modest skill in the art, Tasdighi and Yamauchi entirely fail to disclose all the limitations recited in Claim 12.

Remarks regarding the phrase *Substantially Sine-Like* that are set forth below in respect of rejections of claims as indefinite (*see* subsection *VII.C.1.b Rejection of Claims 12, 20 and 28 as Indefinite*) are also entirely applicable here, and are accordingly incorporated here by reference. In brief, when "substantially" is used with a precise relationship, the relationship is readily understood. For example, the court in *Andrew Corp. v. Gabriel Electronics,* 847 F.2d 819, 822, 6 USPQ2d 2010 (Fed. Cir. 1988)[11] held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." "Substantially sine-like" is not less precise than "substantially equal ... illumination patterns."

In view of the facts and law identified in the remarks set forth above, neither Tasdighi, nor Yamauchi, nor the combination of the two, can fairly be said to disclose all of the limitations of Claim 12. This combination of references thus fails to establish *prima facie* obviousness of Claim 12. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 12.

VII. B.1.g Rejection of Claims 14 and 16 over Tasdighi in view of Yamauchi

Claims 14 and 16 depend from Claim 12, and are nonobvious over Tasdighi in view of Yamauchi for at least the reasons set forth above with respect to Claim 12. They may stand or fall with Claim 12.

VII. B.1.h Rejection of Independent Claim 28 over Tasdighi in view of Yamauchi

Claim 28 is a method claim that is related to the apparatus Claim 12. Claim 28 recites in part (underlining added for emphasis): "b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions such that a voltage of the first charge pump clock output is substantially sine-like." The remarks set forth above to support a conclusion of nonobviousness for Claim 12 over Tasdighi in view of Yamauchi apply *mutatis mutandis* (indeed, with very little adjustment) to support a conclusion that Claim 28, as presently pending, is nonobvious over Tasdighi in view of Yamauchi. Neither of these references teaches, discloses, or fairly suggests the underlined limitation. As such, the combination fails to establish *prima facie* obviousness of Claim 28. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 28.

VII. B.1.i Rejection of Claims 29-33, 36 and 40 over Tasdighi in view of Yamauchi

Each of Claims 29-33, 36 and 40 is nonobvious over Tasdighi in view of Yamauchi for at least the reasons set forth above in regard to the rejection of Claim 28 over this combination of references. Claims 29, 33 and 36 will stand or fall with Claim 28. The following claims are nonobvious over Tasdighi in view of Yamauchi for additional reasons, as set forth below.

Claim 30: In addition to the limitations of Claim 28, Claim 30 further includes the limitations of Claim 29 plus those additionally recited in Claim 30. Claim 30 recites in part "the first charge pump clock output is the second charge pump clock output." Substituting into the limitations of Claim 29 accordingly, Claim 30 includes the following effective limitation further to those of Claim 28 (underlining added for emphasis): "coupling the TC to the source voltage via a charging TCCS circuit, under control of the first charge pump clock output, during charge periods that nonoverlappingly alternate with the discharge periods." Neither Tasdighi nor Yamauchi disclose this limitation.

Although an obviousness rejection under 35 USC 103 may be supported by disclosure in a plurality of references, the standard for disclosure is not reduced as compared to rejections under 35 USC 102. A limitation is not disclosed at least unless the descriptive matter of the combined references includes the claimed limitation in as much detail as is contained in the claim. "The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson, id.*, endnote 2. Neither Tasdighi nor Yamauchi disclose any detail as to the number of clock outputs, or any detail of the coupling between the clock outputs and the transfer capacitor coupling switches. As such, they fail to disclose the recited limitation as required for a rejection under 35 USC 103, and thus fail to establish *prima facie* obviousness of Claim 30 for this additional reason. The rejection of Claim 30 over Tasdighi in view of Yamauchi is therefore improper for this additional reason, and, as such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 30.

Claim 31: Claim 31 depends from Claim 30, and is thus nonobvious over Tasdighi in view of Yamauchi for all of the reasons set forth above in regard to Claims 28 and 30. Claim 31 recites in part (underlining added for emphasis): "... controlling all TCCS circuits by means of the first charge pump clock output." This constitutes yet further detailed limitation on the nature of the clock outputs (single), and on their coupling to the TCCS circuits. Irrespective of the nonobviousness of Claim 30, neither Tasdighi nor Yamauchi disclose this further detailed limitation, and Claim 31 is accordingly nonobvious over this combination of references due to their failure to disclose the further limitation recited in Claim 31. The rejection of Claim 31 over Tasdighi in view of Yamauchi is therefore improper for this additional reason, and hence the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 31.

Claim 32: Due to depending from Claim 31, Claim 32 is nonobvious over Tasdighi in view of Yamauchi for all of the reasons set forth above with respect to Claims 28, 30 and 31. However, Claim 32 recites the following further limitation (underlining added for emphasis): "... coupling the TC to a connection of the source voltage during a charging period via the charge pump clock output." The Examiner's statement in support of this ground of rejection is set forth on page 21, lines 16-19 of the Final Office Action, and reveals the same error as is remarked upon above in subsection *VII.B.1.b Rejection of Claims 2-4 and 10 over Tasdighi in view of Yamauchi* with respect

to Claim 10, which includes a similar limitation. The Examiner apparently fails to recognize that "via" means "through," and instead suggests that the limitation is disclosed if the TC is coupled to a connection of the source voltage under control of the charge pump clock output. In any event, both Tasdighi and Yamauchi entirely fail to disclose this very particular limitation in respect of the coupling between the charge pump clock and the TC. As such, the combination of references fails to establish *prima facie* obviousness of Claim 32 for this further reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 32.

Claim 40: Claim 40 is nonobvious over Tasdighi in view of Yamauchi for all of the reasons set forth above with regard to Claim 28. Claim 40 recites in part (underlining added for emphasis): "... generating the first charge pump clock output by means of a current-starved ring oscillator including not more than three inverting driver sections coupled in a ring." This limitation is similar to the limitation of Claim 43 discussed above (*see* subsection *VII.B.1.c Rejection of Independent Claim 43 over Tasdighi in view of Yamauchi*). As such, Claim 40 is nonobvious over Tasdighi in view of Yamauchi, irrespective of the nonobviousness of Claim 28, for at least the same reasons set forth in subsection *VII.B.1.c* (incorporated here by reference) to support a conclusion that Claim 43 is nonobvious over the cited combination of references.

Further analysis buttressing a conclusion that three-stage current starved ring oscillators are contrary to charge pump prior art: The following remarks provide additional reasons, somewhat more succinct than those set forth in subsection *VII.B.1.c*, supporting a conclusion as to the patentable distinction conferred by the additional above-underlined limitation of Claim 40.

The proportion of the oscillation period that is occupied by transitions between "high" and "low" in a current-starved ring oscillator depends upon the number of inverter stages employed. The total period of the oscillator output increases in direct proportion to the number of stages, while the duration of the transitions remain essentially constant (for given FET gate thresholds). A constant transition time becomes a progressively smaller fraction of an increasing period. Conversely, the transition time occupies the largest proportion of the current-starved ring oscillator having the smallest number of stages, making the output of such ring oscillators the least "square" for a given design.

Hara is the only reference of record that provides information as to the magnitude of the number of stages that should be used in implementing ring oscillators in a charge pump, and specifically recommends that only current-starved ring oscillators having five or more stages be used. Hara does not explain the basis for the recommendation, but an inference may be drawn from three items of circumstantial evidence: (1) no prior art reference (of record) indicates a clock waveform that is significantly less square than that of Hara's five-stage ring current starved ring oscillator (Chern has a maximum transition/period ratio 9% larger than Hara); (2) the waveform becomes progressively less square as the number of inverter stages declines, and (3) Hara recommends only against using the very fewest number of inverter stages in a current-starved ring oscillator for a charge pump. The fair inference to be drawn from these facts is that three (or less) staged current-starved ring oscillators create a waveform that is not sufficiently square for use with a charge pump. That is consistent with the fact, based on a survey of the prior art of record as noted above, that all propose waveforms that are square or nearly square.

Accordingly, the explicit teaching, in Hara, that current-starved ring oscillators are suitable for charge pumps only if they have five or more inverter stages, buttresses the evidence of the other prior art of record to support a conclusion that those of skill in the charge pump arts avoided clocks that are not sufficiently square enough.

The remarks above support a conclusion that Claim 40 is thus nonobvious over Tasdighi in view of Yamauchi for significant additional reasons. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 40.

VII.B.1.j Rejection of Claims 19 and 20 over Tasdighi in view of Yamauchi

Claims 19 and 20 depend from Claim 18, and are accordingly nonobvious over Tasdighi in view of Yamauchi for at least the same reasons that this combination of references fails to render obvious Claim 18. Accordingly, it is necessary first to compare Tasdighi and Yamauchi against the requirements of Claim 18.

The failure of Tasdighi to disclose the missing descriptive matter identified in subsection *VII.A.1.a Missing Descriptive Matter* is demonstrated in detail in subsection *VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi*, incorporated here by reference. Yamauchi arguably

provides sufficient detail to suggest a "single-phase clock." However, a single-phase clock source is meaningless if such clock source is split into a plurality of phases before being coupled to the TCCSs (transfer capacitor coupling switches, or bridge switches). The single-phase clock output, as required by Claim 18, must remain single until it is coupled to all of the TCCSs. Thus, the requirements for a single-phase clock work together with the requirements for passive coupling to the TCCSs, and showing one piece of that combination has no bearing on the novelty of the claimed invention.

As to all of the rest of the missing descriptive matter, Yamauchi teaches no coupling details whatsoever, and even fails to disclose TCCSs at all. In particular, both Tasdighi and Yamauchi teach nothing whatsoever in regard to coupling of the clock to the TCCSs. They thus fail to provide evidence of any coupling limitations at all. These references certainly cannot fairly be conjectured to somehow teach coupling that is contrary to other prior art that shows such details. There is overwhelming reason to believe that the prior art invariably uses either plural-phased clocks, or else generates plural phases from a single clock source (*see* subsection *VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi*).

Yamauchi is entirely unable to remedy the omissions of Tasdighi as to any significant part of the missing descriptive matter remarked upon in subsection *VII.A.1.a Missing Descriptive Matter* (the remarks above demonstrate that a single-phase clock, by itself, is insignificant). As such, the combination of Tasdighi with Yamauchi entirely fails to support *prima facie* obviousness of Claim 18, for substantially every reason set forth in subsection *VII.A.1.a.*

Although the Examiner does not reject Claim 18 as obvious over Tasdighi in view of Yamauchi, the clear nonobviousness of Claim 18 over this combination of references confers patentable distinction also on all of the claims, such as 19 and 20, that depend from Claim 18. Claim 20 is not presently argued as having further distinction over these references than does Claim 18, but that is ample distinction. However, Claim 19 is additionally nonobvious over Tasdighi in view of Yamauchi for the reasons set forth below.

Claim 19 recites in part (underlining added for emphasis):

e) a second transfer capacitor;

f) one or more second-source switching devices disposed in series between the second transfer capacitor and a second voltage source; and

g) one or more second-output switching devices disposed in series between the second transfer capacitor and a second output voltage supply;

h) wherein the charge pump clock output is coupled to all of the second-source switching devices to cause conduction during the charge periods and nonconduction during the discharge periods, and is coupled to all of the second-output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods.

To support the rejection of Claim 19 over Tasdighi in view of Yamauchi, the Examiner states (Final Rejection, page 19 beginning line 7, underlining added for emphasis):

> Although the reference(s) read on the limitations of claims 18 and 49 as previously described above, the reference(s) do not show or disclose a second charge pump stage of claim 19, or second TC, second TC charging switch, second output supply, and second TC discharging switch of claim 54. However, it would have been obvious to one of ordinary skill in the art to add a second charge pump stage/apparatus to the charge pump apparatus of claim 18, or add the elements related to the method steps of claim 49. It could have the same basic structure as Tasdighi's Fig. 2, wherein the second charge pump stage could be coupled in parallel to the charge pump apparatus, and both would receive the same charge pump clock output.

The Appellants' representative respectfully submits that, in addition to the unsupported assertion of missing descriptive matter in Tasdighi, the Examiner further conjectures that Tasdighi "could" be coupled as required by Claim 19. That further conjecture is not only unsupported by Tasdighi and Yamauchi, but is unsupported by the entire body of evidence of record, and moreover is contrary to such evidence, as demonstrated by the particularly apposite example of the Bingham '774 reference incorporated by reference in Tasdighi, as set forth below.

Tasdighi's Fig. 2 is a single stage charge pump, and as such entirely fails to provide evidence of the second stage elements recited in Claim 19. However, the Tasdighi reference, in fact, includes a simplified diagram of a two-stage charge pump (FIG. 4). FIG. 4 includes no detail regarding the coupling of the clock to the switches, as is required by Claim 19, and thus does not by itself disclose the recited limitations. However, Tasdighi describes FIG. 4 thus (col. 3 line 45+): "FIG. 4 illustrates a charge pump circuit which is the subject of U.S. Pat. No. 4,897,774 ... incorporated herein by

reference." (In addition to being incorporated by reference in the primary reference that is cited by the Examiner in order to support the obviousness rejection, the Bingham '774 patent was also submitted by the Appellants in an IDS, and has been considered by the Examiner.) The presence of such clearly relevant teaching incorporated (by reference) in the primary reference makes the Examiner's reliance on groundless conjecture very perplexing.

FIG. 1B of Bingham '774 illustrates, with clarity, that the charge pump switches (14a, 16a, 18a and 20a for first TC 10, and 26a, 28a, 30a and 32a for second TC 24) are controlled by two different phase signals 44 and 46 provided by phase control block 42. The phase control block 42 serves as part of the coupling between a charge pump clock and the charge pump switches, as may be seen in FIG. 2. A single output from a clock 56 is actively coupled through six FETs 46, 48, 50, 52, 54 and 56 to generate the two phase signals 44 and 46 that are applied to the switches.

"The clock" of Claim 19 is the single-phase clock of Claim 18 that is "coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices ... the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices." In contrast, Bingham '774 clearly uses two clock phases, developed in the active clock coupling circuitry, to control the source and output switching devices. Thus, "the clock" of Bingham '774 is contrary to the requirements for such clock that are incorporated in Claim 19.

The facts noted above support conclusions (1) that the art cited by the Examiner as rendering obvious Claim 19, Tasdighi and Yamauchi, fails to disclose the additional limitations set forth in Claim 19, and (2) that, furthermore, the cited references in fact incorporate relevant subject matter that is contrary to the limitations of Claim 19. The combination of Tasdighi and Yamauchi thus fails to establish *prima facie* obviousness of Claim 19.

It is worth further noting that the Federal Circuit has been very emphatic that the question is never whether a thing could be done. "That one *could* invent such a cable tie is unquestioned. Caveney *did*. The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made. *Panduit, id.*, endnote 8, emphasis in original). In

view of *Panduit*, it is particularly clear that the Examiner's rejection of Claim 19 over Tasdighi in view of Yamauchi is unsupported and improper. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 19.

VII. B.1.k Rejection of Independent Claim 49 over Tasdighi in view of Yamauchi

Claim 49 recites in part (underlining added for emphasis):

a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

Yamauchi discloses no detail in respect of TC charging or discharging switches, nor of coupling a clock to such switches (TC coupling switches "TCCSs"). Tasdighi itself discloses no detail in respect of a single-phase charge pump clock, or in respect of coupling such clock to TCCSs. Bingham '774, incorporated by reference by Tasdighi, discloses a single-phase charge pump clock 56 (FIG. 2), but teaches that such clock is to be actively coupled to the TCCSs, contrary to the requirements recited in Claim 49. Accordingly, Tasdighi and Yamauchi in combination, even considering material incorporated by reference in Tasdighi, fail to teach all of the limitations of Claim 49, and thus do not support *prima facie* obviousness of Claim 49. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 49.

VII. B.1.l Rejection of Claims 50-51, 53-54 and 57-58 over Tasdighi in view of Yamauchi

Claims 50-51, 53-54 and 57-58 are nonobvious over Tasdighi in view of Yamauchi at least by virtue of depending from Claim 49, which is nonobvious over these references as demonstrated by the remarks set forth above in subsection *VII.B.1.j Rejection of Claims 19 and 20 over Tasdighi in view of Yamauchi*. Claims 50, 54 and 57-58 may stand or fall with Claim 49, but additional reasons are set forth below for the nonobviousness of Claims 51 and 53 over Tasdighi in view of Yamauchi.

Claim 51: In addition to the limitations of Claim 49, Claim 51 incorporates the following limitations "coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output;" and "coupling the TC to a voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." These limitations constitute further detail that is absent from the disclosure of both Tasdighi and Yamauchi, even including the incorporated disclosure of Bingham '774 incorporated in Tasdighi by reference. Tasdighi and Yamauchi themselves are devoid of relevant disclosure. The coupling of a single-phase clock to a plurality of charging TCCSs and a plurality of discharging TCCSs associated with a TC (transfer capacitor) in Bingham '774 is not only active, but it explicitly develops a plurality of different phases that are then connected to the different TCCSs. As such, the combination of Tasdighi and Yamauchi, even further including the incorporated disclosure of Bingham '774, fails to disclose all of the limitations of Claim 51 for these further reasons. Tasdighi and Yamauchi thus fail to support *prima facie* obviousness of Claim 51 for these additional reasons, wherefore the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 51.

Claim 53: Claim 53 recites in part: "coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." This limitation constitutes further detail that is missing from the disclosure of both Tasdighi and Yamauchi. The coupling of a single-phase clock to a plurality of charging TCCSs associated with a TC (transfer capacitor) in Bingham '774 is not only active, but it explicitly includes developing a plurality of different phases that are then connected to the different charging TCCSs. As such, the combination of Tasdighi and Yamauchi, even further including Bingham '774 (incorporated by reference), fails to disclose all of the limitations of Claim 53 for this further reason. Tasdighi and Yamauchi thus fail to support *prima facie* obviousness of Claim 53. Accordingly, the panel is respectfully requested, for this additional reason, to reverse the Examiner as to this ground of rejection of Claim 53.

VII.B.2 Rejections under 35 USC § 103(a) over Tasdighi in view of Hara

On page 22 of the Final Rejection, the Examiner rejects Claims 1-9, 12, 16, 18, 20, 22, 24-41, 43-51, 53-61 and 66-67 as obvious over Tasdighi in view of Hara. Each of these rejections is

respectfully traversed because the cited references fail to provide disclosure sufficient to support *prima facie* obviousness of any of the rejected claims.

Hara is very similar to Yamauchi. Both focus on the clock alone, and show no detail whatsoever, but only a non-electrical arrow, to indicate coupling between the clock and the charge pump circuits (exclusively FIG. 13, arrow from oscillators 89b and 89d to charge pump circuits 89c and 89e, respectively; description of FIG. 13 beginning col. 8 line 44 adds no detail). Hara, like Yamauchi, teaches current-starved type ring oscillators for use with a charge pump (see, *e.g.*, Figs. 1 and 4-6).

Two differences of Hara from Yamauchi warrant comment. First, Hara explicitly supports the Appellants' contention that current-starved ring oscillators for use with charge pumps would not be configured to have as few as three inverter sections coupled in series. Despite the added components, chip real estate, and even drawing clutter, Hara (Figs. 1 and 4-6) always expressly illustrates ring oscillators having five inverter sections. Moreover, Hara describes the number of inverter sections as follows (col. 5 lines 60-62, emphasis added): "Herein, the five stages of inverters are used to constituting [*sic*] the ring oscillator by way of illustration, but odd number stages more than five may be employed." This is strong support for Appellants' above-stated contention. While Yamauchi merely notes that a ring oscillator must have an odd number of inverters to function (a physical limitation), Hara, directed toward oscillator designs for use in charge pumps, actually identifies an appropriate range of ring inverter sizes. Even while endeavoring to be inclusive by explicitly expanding the range of the number of inverters that is deemed suitable, Hara still excludes current-starved oscillators having less than five inverter stages. Thus, Hara quite explicitly teaches away from the Appellants' recited limitation "[A current-starved] ring oscillator comprising an odd number of not more than three inverting driver sections ... ."

Second, Hara contains "prior art" subject matter that was not selected by the inventors because it is relevant to charge pumps. Such prior art subject matter is, instead, general oscillator prior art that is relevant to novel techniques used for controlling the oscillator frequency (because controlling the oscillator frequency is the focus of Hara). Most likely the Japanese Patent Office, as is their practice, required the Hara applicants to add, and comment upon, such prior art, including

Figs. 19 and 20. FIG. 20 is directed to techniques for frequency modulation and provides no teaching remotely relevant to charge pumps. The oscillator shown in FIG. 19 is also not intended for use with a charge pump, but rather is from a patent directed to a phase-locked-loop (PLL) circuit (col. 2 lines 14-16). Hara argues that the circuit of FIG. 19 is not suitable for the purposes of Hara (*i.e.*, for use in a charge pump) (see, *e.g.*, col. 2 lines 48-54). The circuit of FIG. 19 has five inverter stages, but is switchable to employ only three of the five, in order to increase operating frequency. Three-stage ring oscillators are known; but this has no bearing on the obviousness of using such circuits in a charge pump. Conventional charge pump designers have always sought relatively fast-edged clocks (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). Because a three-stage current-starved ring oscillator would not have fast edges, it would not be selected by one of ordinary skill in the art for use in a charge pump. The fact that oscillators for other purposes can tolerate, or even require, sine-like outputs has no bearing on what the person of skill in the charge pump art would have thought was appropriate for controlling a charge pump. The teaching of Hara, as opposed to the foregoing prior art, is intended for use with charge pumps, and Hara indicates that current-starved ring oscillators for charge pumps should have at least five inverter sections.

The remarks above identify the relevant differences between Hara and Yamauchi. Nothing in those differences would remedy the failings of either Tasdighi or Yamauchi to disclose all of the elements of any of the present appealed claims, with the exception of an illustration of a five-stage ring oscillator switchable to operate with three stages. That disclosure is not relevant to charge pumps, being from prior art for general-purpose oscillators (similarly as with Ito, discussed elsewhere). Hara does not submit the illustrated prior art as being relevant to charge pumps, but to the contrary distinguishes it. More importantly, Hara expressly teaches away from "not more than three" stages in such an oscillator for a charge pump, strongly supporting the nonobviousness of claims requiring a current-starved ring oscillator having not more than three inverter stages.

In view of the lack of further material that could remedy any of the failures of Tasdighi and Yamauchi, it is apparent that the combination of Tasdighi with Hara fails to render obvious claims for many of the reasons as does the combination of Tasdighi with Yamauchi. Some brevity will be gained with respect to claims rejected over Tasdighi in view of Hara by referencing the arguments

set forth above with reference to claims rejected over Tasdighi in view of Yamauchi, which can be applied *mutatis mutandis*.

VII.B.2.a Rejection of Independent Claim 1 over Tasdighi in view of Hara

The arguments set forth above in subsection *VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi* are applicable to support a conclusion that Claim 1 is nonobvious over Tasdighi in view of Hara, because Hara provides no more material disclosure than does Yamauchi. Such arguments are hereby incorporated into this subsection by reference.

Claim 1, as presently pending, recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes
>
> i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and
>
> ii)circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output;

On page 15 of the Final Rejection, beginning at line 16, the Examiner acknowledges that Tasdighi does not disclose a ring oscillator with only three sections, or the current-limit requirements of Claim 1, then turns to Hara for disclosure of these elements. As to the requirement for "not more than three inverter driver sections," the Examiner offers the following statement (Final Rejection page 23 beginning line 11): "Using a modified ring oscillator with only three driver sections ... renders claim 1 obvious ... [remarks on current limit requirements] ... A ring oscillator with three driver sections will still provide a charge pump clock output, and will use few elements, require less area, and consume less current, than a ring oscillator with a higher, odd number of driver sections." The Examiner provides fails entirely to provide any evidence that those of skill in the charge pump arts would use three current-starved inverter stages in a ring oscillator for a charge pump clock. Lacking any evidentiary support, the Examiner again resorts to pure conjecture as to what could be

done. The Appellants do not argue that it is impossible, and indeed would not claim it if it were impossible. However, it has conventionally been thought undesirable, as may be deduced by, *inter alia*, the absence of an actual example of such a clock in the prior art, despite the large number of references in this crowded field.

The reason that a current-starved ring oscillator of only three sections helps solve the Appellants' problem of avoiding noise generation is precisely the reason that they have been avoided in conventional charge pumps: such a ring oscillator produces a clock output having very non square-like edges. The conventional wisdom of charge pumps, as may be seen in the teaching of all of the references that are of record in this application, is that charge pump clocks should have edges that are as sharp as is conveniently possible to reduce uncertainty in timing and thereby ensure that switches are turned on for as long as possible without causing concurrent conduction of switches that are disposed in series across a supply or a transfer capacitor (see, *e.g.*, US Patent 5126590 to Chern, col. 1 lines 19-27; and US Patent 6518829 to Butler teaches square-edged clocks despite being directed to solving the problem of lowering noise, see abstract and Figs. 3-6). While all voltage transitions take finite time to occur, the prior art consistently teaches generating relatively square waveforms (*See* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*).

The problem with using only three stages in current-starved ring oscillators, from the conventional standpoint, is that they do not produce output waveforms that are sufficiently rectangular. Increasing the number of inverter stages in a current-starved ring oscillator decreases the proportion of the output period that is required for each transition between low and high levels, thus increasing the "squareness" of the output waveform.

> A note about waveform descriptive terminology: "Square", "square-like", and "rectangular" are employed herein interchangeably to describe essentially identical waveform shapes. These terms are equivalent as a practical matter, because with the proper scaling (of time and amplitude units), any rectangular wave becomes a "square" wave. Because there is no inherent numerical relationship between voltage amplitude and time, such scaling in an illustration is essentially arbitrary. Changes to such arbitrary scaling do not change the information conveyed by the illustration. "Rectangular" is generally preferred because it avoids a need to scale an illustration, but engineers commonly refer to "square" waves or the "squareness"

> of a waveform to convey a waveform that predominantly has only two values (low and high voltages), and which transitions between these two states in a small fraction of the time period of the waveform. "Square" is preferred in some cases. For example, the term "squareness" is less awkward than the alternative term "rectangularity."

As far as using current-starved ring oscillators with charge pumps, Hara explicitly teaches using five inverter stages or more (col. 5 lines 60-62). This is consistent with the conclusion (*See* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*) that relatively square clock waveforms have consistently been desired for prior art charge pumps. The output transitions of a five-stage current-starved ring oscillator will occupy a much smaller percentage of the period of the signal; *i.e.*, they will be much more "square."

As noted above, to establish *prima facie* obviousness, all claim limitations must be taught or suggested by the prior art. "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson, id.*, endnote 7. Hara and Tasdighi both fail to suggest the limitation directed to "not more than three inverter driving sections" as recited in Claim 1. As such, the combination of these references does not support *prima facie* obviousness of Claim 1.

At least for the reasons set forth above, Claim 1 is nonobvious over the combination of Tasdighi and Hara. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 1, and as to Claims 2-9 that depend therefrom.

VII.B.2.b Rejection of Claims 2-9 over Tasdighi in view of Hara

Claims 2 and 9 may stand or fall with Claim 1. Claims 3-8 are each further distinguished over a combination of Tasdighi and Hara for the reasons set forth below.

Claims 3 and 4: When a signal is digitally processed, or goes through one or more gain stages, the dv/dt of the signal is likely to be increased. In some instances, resonant circuitry can also raise the dv/dt of a signal. Claim 3 recites in part (underlining added for emphasis): "coupling circuitry configured to couple the particular charge pump clock output as a signal to each of the transfer capacitor coupling switches without increasing a rate of voltage rise or fall of the signal." Claim 4 includes a very similar element.

As noted above, Tasdighi and Hara include no detail regarding coupling, and thus cannot literally disclose such an element. Moreover, far from such a limitation being inherent, the prior art of record teaches away from the underlined limitation. As noted above, the prior art of record teaches that the typical coupling of single clock outputs to a transfer capacitor switch (TCCS) is active, digital device coupling, which would increase the rate of voltage rise or fall of the signal. This would be particularly true if the signal originated in a three-stage current-starved ring oscillator, because such signal would be relatively slow. Tasdighi, even combined with Hara, thus fails to disclose this additional element. The combination of references thus fails to establish *prima facie* obviousness of either of Claims 3 or 4 for this additional reason.

Claim 5: As noted above in, *e.g.*, subsection *VII.B.2.a Rejection of Independent Claim 1 over Tasdighi in view of Hara*, Hara discloses no further subject matter in respect of coupling between a charge pump clock and charge pump switches than does Tasdighi, and thus cannot remedy the omission of elements from Tasdighi to render obvious Claim 5. Claim 5 recites in part: "a capacitive coupling circuit configured to couple one of the at least one charge pump clock outputs to a control node of one of the plurality of transfer capacitor coupling switches." As noted above in subsection *VII.A.1.a Missing Descriptive Matter*, Tasdighi entirely fails to provide disclosure of any such coupling details. Far from being inherent, active and/or logic-gate coupling alternatives are common. As such, Tasdighi in view of Hara cannot fairly be said to disclose this claimed limitation, thus rendering Claim 5 nonobvious over the cited combination of references for this additional reason. Reversal of the Examiner is therefore respectfully requested as to this rejection of Claim 5.

Claims 6 and 7: Compared to Claim 5, Claim 6 includes more detailed requirements for the coupling between clock and TCCSs, and thus is additionally patentable over Tasdighi in view of Hara for even more reasons than is Claim 5. Claim 6 recites in part (underlining added for emphasis): "capacitive coupling circuits to couple a control node of each of the plurality of transfer capacitor coupling switches to the particular charge pump clock output." No evidence of record supports the Examiner's contention that Tasdighi can fairly be said to disclose these limitations, and Hara provides no disclosure to remedy the deficiency of Tasdighi. Thus, Claim 6 is nonobvious over Tasdighi in view of Hara for these further reasons, and Claim 7 is nonobvious at least by virtue of properly depending from Claim 6. Claim 7 may stand or fall with Claim 6.

Claim 8: Claim 8 is nonobvious over Tasdighi in view of Hara by virtue of properly depending on Claim 5. Claim 8 recites in part: "[T]he capacitive coupling circuit does not conduct substantial charge to the transfer capacitor." This limitation excludes a whole category of charge pumps, such as those that connect the transfer capacitor directly to a clock output and thus conduct transfer current through the clock output, and through the coupling capacitor. In such circuits, the coupling capacitor is the transfer capacitor. This further detail is yet another required feature that is disclosed in neither Tasdighi nor Hara, and as such renders this reference combination unable to establish *prima facie* obviousness of Claim 8 for this further reason.

VII.B.2.c Rejection of Independent Claim 43 over Tasdighi in view of Hara

Claim 43 is a method claim corresponding generally to Claim 1. In particular, Claim 43 requires (underlining added for emphasis): "b) limiting source current provided to each inverting driver output node of a current-starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator." The arguments set forth above in subsection *VII.B.2.a Rejection of Independent Claim 1 over Tasdighi in view of Hara* are directly applicable, and are incorporated here by reference. Tasdighi does not disclose any oscillator details beyond suggesting a ring oscillator. Hara does suggest both a particular desirable number of stages of current-starved inverters in a ring oscillator for a charge pump, and a range of the number of stages that is appropriate. The number suggested is five inverter stages (Figs. 1 and 4-6), and the range suggested is five or more such inverter stages (col. 5 lines 60-62). Thus, Hara not only lacks description of using three inverting stages in a ring oscillator for a charge pump, but actively teaches away from the limitations of Claim 43. As noted above, Hara teaches that five or more, not three or less, inverting stages be used in ring oscillators designed for use in charge pumps. As such, Hara clearly supports the Appellants' contention that Claim 43 is nonobvious over Tasdighi in view of Hara. Tasdighi, even combined with Hara, thus fails to establish *prima facie* obviousness of Claim 43. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 43.

VII.B.2.d Rejection of Claims 44-48 over Tasdighi in view of Hara

Claims 44-48 include all of the limitations of Claim 43, and are nonobvious over Tasdighi in view of Hara for at least the reasons set forth above. Claim 44 may stand or fall with Claim 43.

"Fact finding by the USPTO is subject to review by the Federal Circuit under standards of review established by the Administrative Procedure Act (APA). "In accordance with the APA, agency factual findings are sustained unless they are arbitrary, capricious, or unsupported by substantial evidence ... " *Energizer Holdings, Inc. V. International Trade Commission*, 435 F.3d 1366 (Fed. Cir. 2006)(endnote 21).

The Examiner declines to explicitly indicate evidence to support this ground of rejection of Claims 44-48 (see Final Rejection, page 27 lines 3-7), relying instead on "the same reasoning as previously presented with respect to the other rejected claims." However, nowhere in the Final Rejection does the Examiner present any reasoning for rejecting Claims 45-47. Such absence of evidence is less than "substantial evidence." The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claims 45-47 for failing to meet the "substantial evidence" requirement set forth by the APA. Improperly supported or not, this ground of rejection has been retained in the Final Rejection, and as such the Appellants are required to respond to it. Reasons supporting the nonobviousness of Claims 45-48 over Tasdighi in view of Hara, further to those that support the nonobviousness of Claim 43 over these references, are therefore set forth below .

Claim 45: Claim 45 depends from Claim 43, and further requires (underlining added for emphasis): "coupling a capacitor to the driver output node of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node." Neither Tasdighi nor Hara disclose, teach or fairly suggest such an element. As such, the cited references fail to teach all of the limitations of Claim 45, thus further failing to support *prima facie* obviousness of Claim 45 for this further reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 45 at least for this further reason.

Claim 46: Claim 46 depends from Claim 43, and further requires: "coupling the first charge pump clock output to a control node of the discharging switch and/or to a control node of a charging

switch via a corresponding capacitive coupling circuit." This requirement further distinguishes Claim 60 from Tasdighi in combination with Hara.

The Examiner acknowledges that this requirement is not shown by either reference (see Final Rejection page 24 lines 3-4). Instead, the Examiner relies on an assertion that a skilled person would choose to modify Tasdighi in this manner simply because capacitors are known to be a possible way to couple circuits.

No motivation is seen or even proposed by the Examiner for employing a coupling capacitor in this manner. In making the rejection for obviousness, the Examiner points to a capacitor used in a background reference of Hara for a purpose that is completely unrelated to charge pumps, namely FM modulating an analog input signal (see Hara, Fig. 20 and col. 2 lines 67-68). The Examiner fails to offer any motivation as to why a skilled person in the charge pump art might choose to use such a capacitor for the purpose recited in Claim 46. The Examiner states only (Final Rejection page 24 lines 3-9; underlining added for emphasis):

> Fig. 20 of Hara shows capacitive coupling circuits (not labeled) connected to transistors 12p and 12n, which one of ordinary skill in the art would understand are types of coupling switches [*sic*, devices]. Therefore, it would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Hara's clock output OUT and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering Claims 5-6 obvious.

(The Examiner declines to explicitly support his rejections of Claim 43-51, 53-61 and 66-67 over Tasdighi in view of Hara, see Final Rejection page 27 lines 3-7, and the rationale with respect to Claims 5-6 set forth above is the most relevant previous rationale presented by the Examiner.)

The Examiner misleadingly implies that the first sentence provides support for the conclusion by stating "Therefore it would have been obvious ..." However, the conclusion is a legal *non sequitur*. The fact that Hara uses capacitors for unrelated purposes does not constitute motivation to use them in other circumstances (such as required by Claim 46). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)[12] Furthermore, the Federal Circuit disapproves unwarranted assertions of motivation to

combine. "In the first place, the level of skill in the art is a prism or lens through which a judge or jury views the prior art and the claimed invention. This reference point prevents these deciders from using their own insight or, worse yet, hindsight, to gauge obviousness." *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324, 50 USPQ2d 1161 (Fed. Cir. 1999)[13]. The Examiner's conclusory recitation of obviousness does not satisfy the "substantial evidence" requirement of the APA to support this ground of rejection (*Energizer, id.*, endnote 21).

Substantial evidence suggests that capacitively coupling a clock to TCCSs is undesirable for integrated charge pumps of the "control only" family, such as Tasdighi. The Examiner's conclusory statement contradicts the evidence from the relevant prior art that is of record. A great deal of relevant prior art is available in this crowded field. The references of record are only a portion of the available prior art, but are believed to fairly represent the relevant prior art in this regard. The Examiner has searched for this specific element of coupling because it is required by independent Claims 24 and 60. All of the prior art of record is tellingly contrary to the Examiner's unsupported contention that such coupling is obvious in "control only" charge pumps, such as that of Tasdighi. In such "control only" charge pumps, the clock only controls the TCCSs that couple the TC to one supply or another, none of the prior art of record uses capacitive coupling. Instead, they rely on active or direct coupling. Integrated circuit designers use capacitors sparingly, in part because they consume valuable chip real estate, and in part because smaller active devices offer great flexibility for precise control of voltages and timing.

Regardless of the reason, the relevant prior art that is of record provides substantial evidence that skilled charge pump designers avoid capacitive coupling of clock to actively-controlled TCCSs. The prior art of record relevant to such coupling is that which illustrates a bridge-type or "control only" type charge pump, such as Tasdighi's, and which further includes sufficient detail to determine whether the coupling between the clock and the TCCSs is capacitive. The relevant prior art of record is believed to consist of the following (relevant figures indicated parenthetically):

Bingham '577 and Bingham '774 (Fig. 2, clock 56 and FETs 44-54), Nork (Fig. 4A, clock 25 and gate 60; Fig. 8A, clock 25 and FETs 121-124), Butler (Fig. 1, and Figs. 2-3, FETs 68,70,74,76)

Yokomizo (Figs. 1-5, osc. 13 and inverter 32), and non-patent reference "Charge Pumps Shine in Portable Designs" (Fig. 5, oscillator and inverter).

All of the foregoing prior art relevant to coupling of the driver output node to the charge pump employ active devices to develop secondary clock signals or phases that have different, characteristics, such as an inverted voltage. Capacitive coupling is not seen, and would be superfluous in view of the active signal conditioning that is indicated. Thus, all of the references indicated above support a conclusion that the Examiner's proposed circuit (achieved by combining the Tasdighi and Hara references) is not only unmotivated, but is contrary to the practice of those skilled in the art. Lacking this essential component of *prima facie* obviousness, Tasdighi in combination with Hara fail to render Claim 46 obvious. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 46.

Claim 47: Claim 47 depends upon Claim 45, and further includes limitations similar to those recited in Claim 46. As such, Claim 47 is nonobvious over Tasdighi in view of Hara for all of the reasons set forth above for each of those claims. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 47.

Claim 48: Claim 48 recites in part (underlining added for emphasis): "further comprising coupling the first charge pump output as a signal to a control node of the discharging switch circuit via a network that is not configured to increase rates of voltage change of the signal." This element is similar to the elements recited in Claims 3 and 4. The arguments set forth above in subsection *VII.B.1.b Rejection of Claims 2-4 and 10 over Tasdighi in view of Yamauchi* with respect to Claims 3 and 4 is therefore applicable, and supports a conclusion that Claim 48 is nonobvious over Tasdighi and Yamauchi in view of this element. Tasdighi and Yamauchi both fail to teach, disclose or fairly suggest the recited element of Claim 48, especially as underlined above.

As far as any disclosure is shown related to coupling of clocks to charge pump switches, each cited reference provides the same thing: a mere arrow, which conveys no electrical significance, pointing from one block to another. Further, the missing descriptive matter is not inherent, because numerous alternative methods for coupling are possible and indeed common, such that the element is not necessarily included in either reference. In view of the absence of at least this limitation of

Claim 48, the combination of Tasdighi and Yamauchi fails to sustain *prima facie* obviousness of Claim 48 even if only for this reason. Claim 48 is thus properly allowable over these two cited references irrespective of the allowability of Claim 43. Consequently, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 48 as unsupported.

VII.B.2.e Rejection of Independent Claim 12 and Claims 14-17 over Tasdighi in view of Hara

Claim 12 recites in part (underlining added for emphasis):

c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to

i) circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and

ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

To support the rejection of Claim 12 over Tasdighi in view of Hara, the Examiner contends as follows (Final Rejection, page 24 beg. line 15): "Interpreting Hara's Fig. 6 charge pump clock generating circuit in a different manner ... ." (Continuing on page 24, last line, underlining added for emphasis): "Also, since clock output OUT can be considered substantially sine-like (e.g. alternating between high and low type levels), this interpretation renders obvious claim 12."

This statement by the Examiner in support of rejecting Claim 12 over Tasdighi in view of Hara differs very little from the Examiner's statement in support of rejecting Claim 12 over Tasdighi in view of Yamauchi. Hara adds no descriptive material, beyond that provided by Tasdighi or Yamauchi, which is relevant to the limitations of Claim 12 as set forth above, especially to those limitations that are underlined. As such, remarks defending the nonobviousness of Claim 12 over Tasdighi in view of Yamauchi, and remarks defending the definiteness of "substantially sine-like" (subsection *VII.B.1.f Rejection of Independent Claim 12 over Tasdighi in view of Yamauchi* and subsection *VII.C.1.b Rejection of Claims 12, 20 and 28 as Indefinite*), all apply to this cumulative ground of rejection of Claim 12 *mutatis mutandis*, and are incorporated here by reference to support a conclusion that Claim 12 is properly patentable over Tasdighi in view of Hara.

There is one difference in this otherwise cumulative ground of rejection that must be pointed out. The Examiner's parenthetical explanation quoted above appears to imply that "substantially sine-like" merely means "alternating between high and low type levels." This implication may result from an error of logic: while sine waves do alternate between high and low levels, it does not follow that anything that alternates between high and low levels is substantially sine-like. As a reasonable analogy, every normal human has a head with two eyes. However, it does not follow that any animal (or thing) having a head with two eyes "can be considered substantially" human. Indeed, no rational person would say that a hippopotamus is "substantially human-like."

A person of skill in the relevant arts who is unable to distinguish waveforms that are "substantially sine-like" from those that are "substantially rectangular" or between "substantially sine-like" (as claimed) and "a train of pulses" (as described in Tasdighi), would be akin to a zoologist being unable to distinguish animals that are "substantially human-like" from those that are "substantially dog-like." In both cases there are certainly similarities (both waveforms vary between relatively high and relatively low levels; both animals have a head and a torso), but the profound differences are unmistakable to those of skill in the pertinent art.

Otherwise, the Examiner's rejection of Claim 12 as obvious over Tasdighi in view of Hara is simply improper for failing to establish even *prima facie* obviousness of Claim 12, because neither Hara nor Tasdighi disclose, teach or fairly suggest at least the limitation to "substantially sine-like." As such, Claim 12 is nonobvious over this combination of references, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 12.

Claims 14 and 16-17 may stand or fall with Claim 12.

Claim 15: Claim 15 additionally requires "one or more capacitive coupling networks configured to couple one of the at least one charge pump clock outputs to a control node of an active switch." The Examiner supports this ground of rejection of Claims 14-15 and 17 by mere reference to his rejections of Claims 5-6 (and of claims 7-9). His relevant statements seem to begin on page 24 at line 3 of the Final Rejection. Those statements acknowledge that neither reference shows capacitive coupling to a TCCS, but assert: "Fig. 20 of Hara shows capacitive coupling circuits (not labeled) connected to transistors 12p and 12n, which one of ordinary skill in the art would

understand are types of coupling switches. Therefore, it would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Hara's clock output OUT and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1, SW2 or 26, 27) of Tasdighi, thus rendering [the claims] obvious."

With all due respect, the Examiner mischaracterizes Hara. A skilled person would certainly not understand transistors 12p and 12n to be "types of coupling switches," for they are not switches at all. They are employed as current limit devices. Furthermore, the capacitors couple transistors 12p and 12n to an analog control signal in order to modulate the current through the transistors so as to thereby modulate the oscillation frequency of the overall oscillator (see col. 3 lines 3-17, especially lines 3-6). This use of capacitors has no discernable relationship to the digital driving of switching devices that is needed for Tasdighi. Such disparate functionality would certainly not lead one of skill in the art to employ these capacitors in the charge pump circuit of Tasdighi.

The Examiner offers the further motivation (beginning page 24 line 9 of Final Rejection): "The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors." He fails to indicate where the prior art notes that DC blocking is useful or desirable, what transitioning errors might be resolved. This "motivation" is itself conjecture, not provided by any reference indicated by the Examiner, and is a disingenuous attempt to justify what is clearly hindsight analysis. This "motivation" does not satisfy the "substantial evidence" standard required to support a factual claim by the Administrative Procedures Act (discussed elsewhere), and thus cannot support *prima facie* obviousness of Claim 15.

In view of the absence of evidence of motivation, the evidence of the absence of examples of such capacitive coupling to a switch in a control-only charge pump becomes even more compelling. It is observable that the prior art of record fails to suggest or illustrate such coupling of a control signal to a TCCS, and further apparent that the Examiner's search failed to uncover such coupling. The primary reason for this is believed to be that active, digital-type circuitry offers a reduction in integrated circuit space, combined with an increase in circuit flexibility to condition the signals and control their timing, as compared to capacitive coupling. In any event, such active circuitry is noted to be used in all of the relevant prior art of record.

Moreover, Fig. 20 of Hara, upon which the Examiner relies, is not charge pump art at all, but is a ring oscillator for FM-modulating an analog input signal. This has nothing to do with charge pumps. There is simply no motivation for the Examiner's proposed "obvious" substitution.

For the foregoing reasons, as well as all of those set forth in subsection *VII.B.2.l Rejection of Independent Claim 24 over Tasdighi in view of Hara*, the additional element set forth in Claim 15 renders Claim 15 nonobvious over Tasdighi in view of Hara independently of the nonobviousness of Claim 12 from which Claim 15 depends. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 15.

VII.B.2.f Rejection of Independent Claim 28 over Tasdighi in view of Hara

Claim 28 is a method claim that is related to the apparatus Claim 12. Claim 28 recites in part (underlining added for emphasis): "b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions such that a voltage of the first charge pump clock output is substantially sine-like." The remarks set forth above in the preceding subsection *VII.B.2.e* to support a conclusion of nonobviousness for Claim 12 over Tasdighi in view of Hara, including those incorporated by reference, apply *mutatis mutandis* (indeed, with very little adjustment) to support a conclusion that Claim 28, as presently pending, is nonobvious over Tasdighi in view of Hara. All such remarks are therefore incorporated here by reference. Neither Tasdighi nor Hara teaches, discloses, or fairly suggests the underlined limitation. As such, the combination fails to establish *prima facie* obviousness of Claim 28. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 28.

VII.B.2.g Rejection of Claims 29-41 over Tasdighi in view of Hara

Claims 29-41 are nonobvious over Tasdighi in view of Hara for the reasons set forth above, by virtue of depending from Claim 28. Claims 29, 33 and 36-40 may stand or fall with Claim 28. Further reasons for nonobviousness over this reference combination are set forth below with respect to specific claims.

Claim 30: In addition to the limitations of Claim 28, Claim 30 includes the limitations of Claim 29, and further requires that "the first charge pump clock output is the second charge pump

clock output." Substituting into the limitations of Claim 29 accordingly, Claim 30 includes the following effective limitation further to those of Claim 28 (underlining added for emphasis): "coupling the TC to the source voltage via a charging TCCS circuit, under control of the first charge pump clock output, during charge periods that nonoverlappingly alternate with the discharge periods." Neither Tasdighi nor Yamauchi disclose this limitation.

Although an obviousness rejection under 35 USC 103 may be supported by disclosure in a plurality of references, the standard for disclosure is not reduced as compared to rejections under 35 USC 102. A limitation is not disclosed at least unless the descriptive matter of the combined references includes the claimed limitation in as much detail as is contained in the claim. "The identical invention must be shown in as complete detail as in the patent claim." *Richardson, id.*, endnote 2. Neither Tasdighi nor Hara disclose any detail as to the number of clock outputs, or any detail of the coupling between the clock outputs and the transfer capacitor coupling switches. As such, they fail to disclose the recited limitation as required for a rejection under 35 USC 103, and thus fail to establish *prima facie* obviousness of Claim 30 for this additional reason. The rejection of Claim 30 over Tasdighi in view of Hara is therefore improper for this additional reason, and hence the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 30.

Claim 31: By virtue of dependency, Claim 31 is nonobvious over Tasdighi in view of Hara for all of the reasons set forth above in regard to Claims 28 and 30. Claim 31 recites in part (underlining added for emphasis): "... controlling all TCCS circuits by means of the first charge pump clock output." The cited references both fail to teach or fairly suggest this further detailed limitation on the nature of the clock outputs (single), and on their coupling to the TCCS circuits. Claim 31 is accordingly nonobvious over Tasdighi in view of Hara for this additional reason, so the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 31.

Claim 32: Due to depending from Claim 31, Claim 32 is nonobvious over Tasdighi in view of Hara for all of the reasons set forth above with respect to Claims 28, 30 and 31. Claim 32 further requires (underlining added for emphasis): "coupling the TC to a connection of the source voltage during a charging period via the charge pump clock output." The Examiner's statement in support of this ground of rejection is set forth on page 21, lines 16-19 reveals the same error as is remarked

upon above in subsection *VII.B.1.b Rejection of Claims 2-4 and 10 over Tasdighi in view of Yamauchi* with respect to Claim 10, which includes a similar limitation. The Examiner apparently fails to recognize that "via" means "through," and instead suggests that the limitation is disclosed if the TC is coupled to a connection of the source voltage under control of the charge pump clock output. In any event, both Tasdighi and Hara entirely fail to disclose this very specific limitation in respect of the coupling between the charge pump clock and the TC. Because the cited references fail to establish *prima facie* obviousness of Claim 32 for this further reason, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 32.

Claim 40: Claim 40 is nonobvious over Tasdighi in view of Hara for all of the reasons set forth above with regard to Claim 28. Claim 40 further requires (underlining added for emphasis): "... generating the first charge pump clock output by means of a current-starved ring oscillator including not more than three inverting driver sections coupled in a ring." This limitation is similar to the comparable limitation of Claim 43 that is discussed above in subsection *VII.B.2.c Rejection of Independent Claim 43 over Tasdighi in view of Hara.* As such, Claim 40 is nonobvious over Tasdighi in view of Hara, irrespective of the nonobviousness of Claim 28, for at least the same reasons set forth in subsection *VII.B.2.c* to support a conclusion that Claim 43 is nonobvious over this combination of references. Those further reasons are incorporated here by reference, for brevity. Hara not only fails to suggest use of a three-stage current starved ring oscillator, he explicitly suggests that five or more stages are required for such oscillators to be used in charge pumps. Claim 43 is thus nonobvious over Tasdighi in view of Hara for significant additional reasons. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 43.

VII.B.2.h Rejection of Independent Claim 18 over Tasdighi in view of Hara

Claim 18 recites in part (underlining added for emphasis): "a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the

output switching devices." Thus, the same single output is required to be coupled to each of the various switching devices.

It is well established that to render a claim obvious, combined references must teach or suggest all of the limitations of the challenged claim. *See, e.g., In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)[14] . Moreover, to be "disclosed" by a reference, limitations must be shown in as much detail as is contained in the claim *Richardson, id.* (endnote 2).

Both Tasdighi and Hara, even considering Bingham '774 (incorporated by reference in Tasdighi), fail to disclose the following: a clock coupled passively to control nodes of source switching devices (a single arrow cannot convey such detail, and the '774 teaches to the contrary); the same clock coupled passively to control nodes of output switching devices (a single arrow cannot convey such detail, and the '774 teaches active coupling to the contrary). Thus, these references fall dramatically short of disclosing all of the limitations of Claim 18 as required by the authorities cited above.

Although some doctrines permit attribution to a reference of literally omitted descriptive matter, all such doctrines are very narrow, and no such doctrine permits attribution of material that is contrary to the weight of the prior art. See the discussion of these doctrines, which include inherency, "common knowledge" and "official notice," that is set forth in subsection *VII.A.1.f Other Doctrines for Asserting Missing Descriptive Material are Also Unavailing.* The missing descriptive material that the Examiner nonetheless attributes to Tasdighi, in particular, is contrary to the evidence of the teaching of the prior art (*see* subsections *VII.A.1.b, VII.A.1.c, and VII.A.1.d* within subsection *VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi*, all of which is incorporated here by reference, for support for the stated conclusion. For the same reasons of law and fact set forth therein, these doctrines do not apply in the present circumstances to permit the Examiner to properly attribute the missing elements from Claim 18 to any of Tasdighi, Hara, Yamauchi, or Ito, none of which literally show the missing elements. Therefore, none of the exceptions that might permit attribution of missing descriptive material apply to sustain the rejection over Tasdighi and Hara over Claim 18.

Moreover, the Examiner has proposed no doctrinal basis whatsoever justifying an attribution of such missing descriptive material to the cited references, but has simply offered conclusory statements. Such conclusory statements are not entitled to evidentiary weight.

The remarks above (including those incorporated by reference) support a conclusion that the combination of Tasdighi and Hara fails to disclose a multiplicity of significant limitations recited in Claim 18. This combination therefore clearly fails to establish *prima facie* obviousness of Claim 18, which is accordingly nonobvious over these cited references. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 18, 20 and 22.

VII.B.2.i Rejection of Claims 20 and 22 over Tasdighi in view of Hara

Claim 22 may stand or fall with Claim 18.

Claim 20 requires (underlining added for emphasis): "circuitry configured ... such that the charge pump clock output voltage is substantially sine-like." As indicated by the prior art of record (*See* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*), persons skilled in the charge pump arts rely upon fast clocks having square or nearly square output waveforms. There is not the least suggestion that sine-like output waveforms are considered even marginally acceptable.

A thorough analysis of the distinction of this limitation over the combination of Tasdighi and Hara is set forth in subsection *VII.B.2.e Rejection of Independent Claim 12 and Claims 14-17 over Tasdighi in view of Hara*. The reasons set forth there are additional reasons supporting patentability of Claim 20, beyond the nonobviousness of Claim 18 from which it depends.

As such, Tasdighi and Hara fail to sustain *prima facie* obviousness of Claim 20 by further reason of its additional limitation. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 20, and indeed as to all claims that include a similar limitation.

VII.B.2.j Rejection of Independent Claim 49 over Tasdighi in view of Hara

Claim 49 recites in part (underlining added for emphasis):

a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively

coupled to a control node of the TC discharging switch and substantially isolated from the TC; and

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

Hara discloses no detail in respect of TC charging or discharging switches, nor of coupling a clock to such switches (TC coupling switches "TCCSs"). Tasdighi itself discloses no detail in respect of a single-phase charge pump clock, or in respect of coupling such clock to TCCSs. Bingham '774, incorporated by reference in Tasdighi, discloses a single-phase charge pump clock 56 (FIG. 2), but teaches that such clock is actively coupled to the TCCSs (creating split phases and thus enabling the device to work properly). Accordingly, Tasdighi and Hara in combination, even considering material incorporated by reference, fail to teach all of the limitations of Claim 49, and thus do not support *prima facie* obviousness of Claim 49. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 49, and as to Claims 50-51 and 53-59 that properly depend from Claim 49.

VII.B.2.k Rejection of Claims 50-51 and 53-59 over Tasdighi in view of Hara

Each of these claims is nonobvious over Tasdighi in view of Hara, for at least all of the reasons set forth above, by virtue of properly depending from independent Claim 49. Claims 57 and 58 may stand or fall with Claim 49. Claims 50-51, 53-56 and 59 are each further distinguished over Tasdighi in view of Hara for the additional reasons set forth below. The Examiner declines to expressly point to evidence supporting this ground of rejection of these claims, stating instead (Final Rejection, page 27 lines 3-7): "Since claims 43-51-, 53-61, and 66-67 are obvious variations of the limitations cited in the numerous claims already rejected within the previous descriptions, it is not considered necessary to keep repeating redundant type explanations. Therefore, claims 43-51, 53-61, and 66-67 are rendered obvious for the same reasoning as previously presented with respect to the other rejected claims." The Appellants cannot deduce the Examiner's evidentiary basis for the rejections from this conclusory statement. Moreover, the Appellants have addressed such previously presented reasoning in the context of the rejections it was written to support. In the absence of a

rationale to respond to, the Appellants merely present ample reasons supporting a conclusion that these claims are properly allowable.

Claim 50: Claim 50 requires: "coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output." Both Tasdighi and Hara fail to disclose, teach or fairly suggest this additional limitation in the level of detail required by Claim 50, as is required to support *prima facie* obviousness (see, *e.g.*, *Richardson*, *id.*, endnote 2). As such, Claim 50 is nonobvious over Tasdighi in view of Hara for this additional reason, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 50.

Claim 51: Claim 51 depends from Claim 50, and hence is nonobvious over Tasdighi in view of Hara for all the reasons applicable to Claim 50. Claim 51 further requires: "coupling the TC to a voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." This further restricts the nature of the coupling between the charge pump clock and the TCCSs, all of which details are undisclosed by either Tasdighi or Hara. As such, the combination of references fails to render Claim 51 obvious by failing to disclose this further limitation. The panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 53: Further to the limitations of Clam 49, Claim 53 requires (underlining added for emphasis): "coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." This limitation defines further detail that is missing from the disclosures of both Tasdighi and Hara, and thus constitutes another limitation that the combination of references fails to teach, disclose, or fairly suggest. Claim 53 is thus nonobvious over Tasdighi in view of Hara for at least this additional reason. The only such details available to this combination of references is found in Bingham '774, but it cannot remedy the deficiency of Tasdighi and Hara because it is contrary to Claim 49, providing not a single-phase clock, but a plural-phase clock to the TCCSs. As such, the combination of Tasdighi and Hara, even further including Bingham '774, fails to disclose all of the limitations of Claim 53 for this further reason. Tasdighi and Hara thus fail to support *prima facie* obviousness of Claim 53, wherefore the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 53.

Claim 54: Further to the limitations of Claim 49, Claim 54 requires

c) coupling a second TC to a second voltage source via a second TC charging switch under control of the charge pump clock output; and

d) coupling the second TC to a second output supply via a second TC discharging switch under control of the charge pump clock output.

These limitations add yet further detail distinguishing Claim 54 from the teaching of Tasdighi in view of Hara. Actually, Tasdighi teaches a two-stage charge pump in Fig. 4; however, the description of Fig. 4 clearly references Bingham '774 for details. Because those details are contrary to the limitations defined by Claim 49 due to a plural-phase clock (or, to the same effect, active coupling of a single-phase clock), the teaching of Tasdighi's Fig. 4 (and Bingham '774) clearly does not render Claim 54 obvious. As to the remaining disclosure of Tasdighi and Hara, there is no teaching or suggestion of all of the limitations of Claim 54 at the level of detail set forth in the claim. Thus, the nonobviousness of Claim 54 is buttressed by the further limitations recited. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 54.

Claim 55: Claim 55 depends from Claim 54, and further requires "coupling the charge pump clock output to a control node of each TC charging switch, and to a control node of each TC discharging switch, via corresponding capacitive coupling circuits." Neither Tasdighi nor Hara discloses this limitation, and the combination thus fails to support *prima facie* obviousness of Claim 55 for this additional reason. The Examiner has declined to specifically identify support for this ground of rejection (see Final Rejection page 27 lines 3-7). Each rationale for rejecting other claims having been addressed with respect to such rejected claims, there is no new rationale for the Appellants to consider and address.

It has previously been demonstrated that a skilled person would in no way be motivated to modify Tasdighi to employ a signal-coupling capacitor that happens to be present in a unrelated FM modulation circuit in Hara. The Examiner does not suggest motivation for such a modification, and none can be found. Moreover, despite the Examiner's earnest search for such subject matter, which is set forth in part in independent Claims 24 and 60, the prior art that is of record fails to yield a single instance in which the clock in a "bridge" or "control only" charge pump, such as is used in

Tasdighi, is capacitively coupled to any of its TCCSs (see the analysis of prior art set forth above in regard to Claim 46 in subsection *VII.B.2.d Rejection of Claims 44-48 over Tasdighi in view of Hara*). This constitutes substantial evidence that one of skill in the charge pump arts would not modify Tasdighi as suggested by the Examiner.

Integrated circuit designers do not insert capacitors in their designs just because it can be done, because capacitors consume substantial area and introduce difficulties with establishing bias. As such, the skilled person would employ active coupling techniques, as shown throughout the prior art, because active couplings are more flexible and consume less integrated circuit real estate. Tasdighi and Hara, in combination, thus fail to sustain *prima facie* obviousness of Claim 55 for these substantial additional reasons. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 55.

Claim 56: Claim 56 is similar to Claim 55, except that it does not depend from Claim 54. With that exception, all of the arguments for further nonobviousness of Claim 55 over Tasdighi in view of Hara are applicable, and incorporated by reference herein to support the further nonobviousness of Claim 56 over that combination of references. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 56 at least by virtue of its additional limitations.

Claim 59: Further to the limitations of Claims 49 and 58, Claim 59 requires (underlining added for emphasis): "limiting rates of both positive and negative voltage transitions at an output node of one of the driver circuits of the charge pump clock generator circuit by coupling a capacitor to the output node of the driver circuit." Neither Tasdighi nor Hara discloses this limitation, which thus renders Claim 59 nonobvious over the combination of references for at least this additional reason. Moreover, as set forth above, it is noted that the prior art suggests that such a modification would be avoided. The prior art of record supports a conclusion that only square or nearly-square clock waveforms were considered suitable for charge pumps. Hara buttresses this conclusion by explicitly indicating that current-starved ring oscillators are suitable for charge pumps only if they have five or more inverter stages (thereby creating more square-like waveforms). The limitation of Claim 59 tends to make the output waveform less square, and thus is contrary to the teaching of the

prior art in regard to charge pump clock outputs. Thus, such a feature is not merely an unmotivated modification of the prior art, but would cause a charge pump clock to be less suitable for its intended purpose. At least for the further reasons set forth above, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 59.

VII.B.2.l Rejection of Independent Claim 24 over Tasdighi in view of Hara

Introductory description of prior art. It should be observed that this field of charge pumps is very crowded. A simple key-word search of the USPTO issued patents since 1975, limited to those having both the terms "charge pump" and "integrated" in their abstracts, returns 216 patent references, of which the vast majority are reasonably relevant. The Examiner has sifted through this prior art. The Appellants' representative has also examined some further prior art references, not yet of record, and found them to be entirely cumulative of those presently of record. (An IDS identifying such additional art will be submitted shortly in satisfaction of Appellants' duty of disclosure, though the references presumably will not be added to the record for purposes of appeal.)

Because the available prior art literature is extensive, it is reasonable to expect to find at least one reference within such literature that discloses each different kind of circuit considered suitable for the common requirement, in control-only charge pumps, of coupling the clock to the TCCSs (transfer capacitor coupling switches). However, none of the references of record (and none of the further references uncovered by Appellants' representative or by the Examiner's search) teach or fairly suggest the charge pump apparatus as set forth in Claim 24. Accordingly, the fact that capacitive coupling, as claimed, has not been found in the relevant art, represents significant evidence that such capacitive coupling is avoided by those of skill in the art.

There are primarily two families of charge pumps, referred to herein as "control only" and "direct drive" (*see* first paragraphs of subsection *V.C Single-Phase Clock Coupled Passively without Transfer Current to TCCSs*). The remarks below address "control only" charge pumps. "Direct drive" charge pumps couple substantial current directly from the clock, through the transfer capacitor (TC), and through TCCSs to source and output supplies. Therefore, "direct drive" charge pumps fail to comport with the requirements, in Claim 24 (b) and (c), that source and output switching devices have control nodes that are isolated from the transfer capacitor. In any event, Tasdighi is an

example of a "control only" charge pump, and the Examiner has not cited "direct drive" charge pumps in this rejection.

The claim: Claim 24 recites in part (underlining added for emphasis):

> a) a transfer capacitor for conveying charge from a voltage source to the output voltage supply;
> b) one or more source switching devices disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;
> c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source; and
> d) a capacitive coupling circuit coupling a charge pump clock output to one of the control nodes corresponding to a source switching device or to an output switching device.

The elements in clauses (a)-(c) generally describe a "control only" charge pump, serving to distinguish this claim from the "direct drive" family of charge pumps. The circuit described by clauses (a)-(c) is generally the type that is disclosed in Tasdighi (though Tasdighi itself does not provide sufficient detail to verify this), and which is illustrated in more detail in Bingham '774 (incorporated in Tasdighi by reference). It is respectfully submitted, however, that clause (d) distinguishes Claim 24 from all prior art examples of such control-only charge pumps.

Discussion of the Rejection: To support his rejection of Claim 24 over Tasdighi in view of Hara, the Examiner points only to "the same reasoning as applied before with respect to the transfer capacitor, source switching device(s), output switching device(s), and the capacitive coupling circuit(s), claims 24-27 are rendered obvious." (Final Rejection, page 25 lines 11-13.) The reasons referred to by the Examiner are thought to be as set forth in the Final Rejection on page 24 beginning at line 3, in respect of claims 6-7. Those reasons acknowledge that neither reference shows capacitive coupling to a TCCS, but assert (Final Rejection, page 24 beginning on line 4): "Fig. 20 of Hara shows capacitive coupling circuits (not labeled) connected to transistors 12p and 12n, which one of ordinary skill in the art would understand are types of coupling switches. Therefore, it would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Hara's clock output OUT and the control node of each corresponding transfer

capacitor coupling switch (e.g. SW1, SW2 or 26, 27) of Tasdighi, thus rendering [the claims] obvious."

It is respectfully submitted that the Examiner mischaracterizes Hara. A skilled person would certainly not understand transistors 12p and 12n to be "types of coupling switches," for they are not employed as switches at all. They are employed as current limiting devices, presumably never either turned on fully or turned off completely, and thus operate in the very conduction region that is avoided, insofar as possible, by a switch. Furthermore, the capacitors couple transistors 12p and 12n to an analog control signal in order to modulate the current through the transistors so as to thereby modulate the oscillation frequency of the overall oscillator (see col. 3 lines 3-17, especially lines 3-6). This use of capacitors has no discernable relationship to the digital driving of switching devices that is needed for Tasdighi. Such disparate functionality would certainly not lead one of skill in the art to employ these capacitors in the charge pump circuit of Tasdighi. Moreover, Fig. 20 of Hara, upon which the Examiner relies, is not charge pump art at all, but is a ring oscillator for FM-modulating an analog input signal (Hara col. 2 line 67 - col. 3 line 9; compared Fig. 19 is also not charge pump art, but PLL art, col. 2 lines 14-16). This has nothing to do with charge pumps.

The Examiner proffers the following as motivation for the proposed modification of Tasdighi (beginning page 24 at line 9 of Final Rejection): "The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors." He fails to offer any evidence that the prior art suggests this motivation, or that the prior art suggests that DC blocking is useful or desirable, or suggests that there are transitioning errors that might thus be resolved. It is apparent, therefore, that the Examiner's proffered "motivation" is pure conjecture, unanchored to the reality of prior art charge pump design. It is difficult to avoid a conclusion that the proffered "motivation" is thus a disingenuous attempt to justify what is clearly hindsight analysis. Due to the lack of evidence for such "motivation," the Examiner's factual conclusion of obviousness (which requires such motivation) fails to satisfy the "substantial evidence" standard. Failing that standard, the Examiner's factual conclusion will not be sustained on appeal to a court. As such, the panel is respectfully requested to discount the unsupported motivation rationale, and to reverse the Examiner's ground for rejection as lacking that required element of *prima facie* obviousness. The substantial evidence standard is set forth in the Administrative Procedures Act, (*see, e.g., Energizer Holdings, Inc. v.*

International Trade Commission, 435 F.3d 1366 (Fed. Cir. 2006)(endnote 21), further cite details unavailable at this time). That motivation is explicitly required to support *prima facie* obviousness is explained, for example, in, *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)[15] There, the court stated:

> We are persuaded that the board erred in its conclusion of *prima facie* obviousness. The question is not whether a patentable distinction is created by viewing a prior art apparatus from one direction and a claimed apparatus from another, but, rather, whether it would have been obvious from a fair reading of the prior art reference as a whole to turn the prior art apparatus upside down. French teaches a liquid strainer which relies, at least in part, upon the assistance of gravity to separate undesired dirt and water from gasoline and other light oils. Therefore, it is not seen that French would have provided any motivation to one of ordinary skill in the art to employ the French apparatus in an upside down orientation. The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification.

In re Gordon, id., endnote 15, at 902, emphasis added.

The reasoning of the court in *In re Gordon* may be applied to the present facts. First, in view of the absence of evidence of motivation, the evidence of the absence of examples of such capacitive coupling to a switch in a control-only charge pump becomes even more compelling. It is observable that the prior art of record fails to suggest or illustrate coupling of a control signal to a TCCS as required by Claim 24, and further apparent that the Examiner's search failed to uncover such coupling. A primary reason for this is submitted to be that active, digital-type circuitry offers a reduction in integrated circuit space, combined with an increase in circuit flexibility to condition the signals and control their timing, as compared to capacitive coupling. In any event, such active circuitry is noted to be used in all of the relevant prior art of record.

The foregoing are reasons pointing away from the proposed modification that are comparable to those weighing against modification in *In re Gordon, id.*, endnote 15. Against that, the Examiner provides not a scintilla of documentary evidence that the prior art contains a motivation to use a

capacitor from an unrelated circuit in a charge pump coupling circuit. Presently, as in *Gordon*, the mere fact that the prior art could be modified as suggested by the Examiner does not support a conclusion of *prima facie* obviousness. Accordingly, the rationale in *Gordon* compels a conclusion that the Examiner should be reversed as to this ground of rejection of Claim 24. Such reversal is respectfully requested.

Notes on the relevant prior art of record: Even within the prior art that happens to be of record, which is merely a fraction of the prior art in this field, there are several examples of "control only" charge pump references of record that include sufficient detail to determine whether such capacitive coupling is used. Those references include US 4777577 (Bingham '577) and US 4897774 (Bingham '774), US 6411531 (Nork), 6518829 (Butler), and 6400211 (Yokomizo). The undersigned has located a number of additional examples in a random perusal of charge pump art that will be submitted shortly in an IDS, but which is presently not of record. Noting that such additional material is not in evidence, the panel is respectfully requested to enter such IDS into evidence if it will help provide further confidence to the conclusions of nonobviousness of, *e.g.*, Claim 24, for none of these examples shows capacitive coupling as claimed in Claim 24. Appellants do not overreach, and would be perfectly content to withdraw claims from appeal if prior art were seen that fairly supported the Examiner's rejections. Further references were considered because, when beginning to prepare this Appeal Brief, Appellants representative became concerned that the Examiner's search might have been inadequate, and that there might actually have been examples in the prior art that would render the claimed invention obvious. The additional random searching of charge pump prior art patents allayed those concerns, but leaves a conundrum: evidence that, though believed fairly cumulative of that already of record, should nonetheless be entered into the record under Rule 56 in caution against the ubiquitous assertions of inequitable conduct during litigation, which evidence in fact reinforces the Appellants contentions, but which cannot of right be entered into the record for purposes of this Appeal.

VII.B.2.m Rejection of Claims 25-27 over Tasdighi in view of Hara

Each of these claims is nonobvious over Tasdighi in view of Hara for the reasons set forth above, by virtue of depending from independent Claim 24. Each is nonobvious for further reasons, as set forth below.

Claim 25: Claim 25 requires "a second capacitive coupling circuit coupling the charge pump clock output to an output switching device control node." Neither of the cited references discloses, teaches or fairly suggests this additional limitation, and thus the combination fails to establish *prima facie* obviousness of Claim 25 for this additional reason. The Examiner declines to provide evidence to support this ground of rejection (see Final Rejection, page 25 lines 11-13). The rationale the Examiner presumably intended to reference is demonstrated, in the immediately preceding subsection, to be inadequate to sustain this ground of rejection. In the absence of new rationale, it is respectfully submitted that this ground of rejection is not properly supported. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 25.

Claim 26: Claim 26 depends from Claim 25, and further requires that "each of the capacitive coupling circuits includes biasing circuitry configured such that an average control voltage causes a switching device to which it is coupled to be substantially nonconductive." This is a very useful limitation that permits control of all TCCSs by a single-phase clock output. The cited prior art does not use capacitive coupling in the manner required by Claim 26. In fact, it is entirely devoid of suggestion or teaching of such biasing considerations. The FETs to which signals are capacitively coupled in Hara are not biased in this manner, but rather are biased to conduct over an entire input voltage range. The absence of teaching or suggestion of this limitation in the cited references is a further reason that Tasdighi and Hara together fail to establish *prima facie* obviousness of Claim 26. Indeed, the rejection of Claim 26 appears to be a mistake, because the Examiner states that Claim 26 would be allowable if properly rewritten in independent form (see Final Rejection, page 30 lines 12-14). To the extent that the Examiner means to maintain this ground of rejection of Claim 26, the panel is respectfully requested to reverse the Examiner.

Claim 27: Claim 27 depends from Claim 25, and is therefore nonobvious over the cited references for all of the reasons set forth above for Claims 24 and 25. Claim 27 further requires that

"all source switching devices disposed in series between the transfer capacitor and the voltage source, and all output switching devices disposed in series between the transfer capacitor and the output voltage, are capacitively coupled to the charge pump clock output." This further coupling detail is not disclosed in either of the cited references, thus precluding *prima facie* obviousness of Claim 27 for this additional reason. Reversal of the Examiner as to this ground of rejection is therefore respectfully requested.

VII.B.2.n Rejection of Independent Claim 60 over Tasdighi in view of Hara

Claim 60 is a method claim directed to subject matter similar to that in Claim 24. In particular, Claim 60 recites in part (underlining added for emphasis):

> a) coupling a first charge pump clock output to a control node of a TC charging switch via a first capacitive coupling network that does not conduct a significant portion of the charge for the output;
> b) coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output;
> c) coupling a second charge pump clock output to a control node of a TC discharging switch via a second capacitive coupling network that does not conduct a significant portion of the charge for the output; and
> d) coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output.

Claim 60, though worded substantially differently than Claim 24, nonetheless is nonobvious over Tasdighi in view of Hara for much the same reasons as is Claim 24. The method defined in Claim 60 is distinguished from the methods of generating output supplies in "direct drive" charge pump circuits by requiring that the capacitive coupling network does not conduct a significant portion of the charge for the output. For the reasons given above with reference to the rejection of Claim 24 over Tasdighi in view of Hara, requirement of coupling charging and discharging switches to charge pump clocks via a capacitive coupling network distinguishes the method of Claim 60 from Tasdighi, even if combined with Hara. As acknowledged by the Examiner, neither of these references discloses such coupling. Moreover, as noted above, no motivation is offered by the Examiner, or found in the references, for modifying the Tasdighi charge pump by substituting

capacitive coupling (performed in Hara for wholly unrelated purposes) for the active coupling taught by Bingham '774 (which is the only detail of coupling provided by Tasdighi, albeit by reference). This combination of the Tasdighi and Hara references accordingly fails to establish *prima facie* obviousness of Claim 60, wherefore the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 60.

VII.B.2.o Rejection of Claims 61 and 66-67 over Tasdighi in view of Hara

Each of these claims is nonobvious over the cited references by virtue of depending from independent Claim 60, and for the following additional reasons.

Claim 61: Claim 61 requires that "the second charge pump clock output is the first charge pump clock output." Neither Tasdighi nor Hara teaches coupling a charge pump clock to TCCSs at a level of detail that permits this requirement to be fairly assumed. Prior art charge pumps, as evidenced by the prior art references of record, always use different clock signals to control the different TCCSs. There is no reason to think that they would not continue to use different clock signals, even if (for some reason) they employed capacitive coupling. Because this limitation cannot fairly be said to be taught or disclosed by either Tasdighi or Hara, Claim 61 is rendered nonobvious over that combination of references for this additional reason.

Claim 66: Claim 66 depends from Claim 60, and further requires (underlining added for emphasis and clarity) "capacitively coupling a control node of each actively controllable TC coupling switch that is incorporated within a charge pump to a corresponding charge pump clock output." For the reasons cited above, the prior art does not teach or fairly suggest that even one such coupling circuit be used. So much less does either the Tasdighi or Hara reference teach, disclose or fairly suggest such uniform use of capacitive coupling circuits. Accordingly, Tasdighi combined with Hara fails to establish *prima facie* obviousness of Claim 66 for this additional reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 66.

Claim 67: Claim 67 is nonobvious over the cited references by virtue of depending from Claim 66, and further requires that "all of the corresponding charge pump clock outputs are a common single-phase output." As noted above with respect to Claim 61, the prior art invariably

employs multiple clock phases for controlling TCCSs in control-only charge pumps such as Tasdighi's. Neither Hara nor Tasdighi teach or suggest to the contrary, nor is there any other reason that a skilled person would couple a single-phase clock to all of the TCCSs. Due to the failure of both Tasdighi and Hara to disclose, teach or fairly suggest this additional limitation, the combination fails to sustain *prima facie* obviousness of Claim 67 for this additional reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 67.

VII.B.3 Rejections under 35 USC § 103(a) over Tasdighi in view of Ito

There is no motivation for combining Ito with Tasdighi. Ito is directed exclusively to Voltage Controlled Oscillators (VCOs), and makes no mention of charge pumps. As such, Ito is devoid of motivation for selecting a particular oscillator for a charge pump. Tasdighi, too, fails to suggest oscillators such as might be taught by Ito, nor does the Examiner point to another source for motivation to make the suggested combination. It is respectfully submitted, and supported by the following remarks, that a skilled person would not consider selecting an oscillator for a charge pump simply because it is an oscillator, but would only select an oscillator having characteristics suitable for a charge pump.

In regard to motivation to combine, the Examiner states (Final Rejection, page 27 lines 17-19): "However, Tasdighi does disclose the clock output of the oscillator can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from [*sic* form] of oscillator" (i.e. see column 5, lines 21-22).

As to the latter point, the form of the oscillator is not in question: it is acknowledged that Hara suggests employing a current-starved ring oscillator with a charge pump. The Appellants' Claim 1, however, requires a current-starved ring oscillator having not more than three inverter stages. The form of the oscillator is not new, but the claimed configuration has heretofore been thought undesirable for charge pumps.

As to the former point, it is true that Tasdighi suggests variations in oscillator design at column 4 lines 47-55. The Examiner neglects to observe, however, that this paragraph is exclusively directed to variations in oscillator design that change the oscillator frequency. (Tasdighi's primary purpose is to operate at reduced frequency to save power when the output load is light: see, *e.g.*, title,

abstract). Tasdighi states (col. 4 lines 36-55, irrelevant details omitted, underlining added for emphasis):

> Oscillator 14 may use conventional techniques to generate a [*sic*] oscillating frequency across terminals 66 and 67. One skilled in the art would understand the numerous varieties of oscillators which may be used in this invention. In conventional oscillators, the frequency of oscillation can be changed by [details of such techniques ...]. It should be understood that changing any parameter of oscillator 14 to adjust the oscillator frequency is envisioned for this invention.

Thus, column 4 lines 47-55 include no suggestion as to the form of the oscillator, or of the oscillator output, or any other reason to select an oscillator. Tasdighi relies on "[o]ne skilled in the art" to select an oscillator appropriate for the charge pump. Both references thus fail to teach or suggest a reason for combining Ito with Tasdighi. As will be demonstrated subsequently, the particular oscillator of Ito that the Examiner submits would obviously be combined with Tasdighi is particularly inappropriate for use with a charge pump.

Oscillators are designed for many very different purposes. When considering an oscillator for a particular purpose, a designer does not choose a random oscillator from those known in the art, any more than a sports car designer, needing a tire design, would select such a tire design at random from the many available. Rather, in both cases the designer considers what type is needed for the purpose at hand. It is true that a tire designed for a sports car can be "changed in many ways," but such latitude simply suggests possible changes within the range of tires that would ordinarily be used with a sports car, and does not amount to a suggestion to use a tire from a substantially different type of vehicle, such as an eighteen-wheeler. Similarly, a person of skill, designing a charge pump, does not consider the entire universe of available oscillators, but rather limits the scope of consideration according to the functionality demanded (in his view) by the charge pump. Thus, the oscillator is chosen to suit the charge pump.

The Ito reference is directed exclusively to voltage-controlled oscillators, particularly for use in phase-locked loops (PLLs; see, *e.g.*, col. 1 lines 8-13). Ito is devoid of any suggestion of the suitability of oscillators for use with charge pumps. As such, there is simply no motivation to combine Ito with Tasdighi, or any other prior art that is directed to charge pumps. To determine a

suitable oscillator, the charge pump designer looks to charge pump art, and to the characteristics of oscillators that have been found suitable there.

The Examiner does not expressly suggest any motivation for making the asserted combination. His statement that "Tasdighi does disclose the clock output of the oscillator can be changed by various ways" might have been intended to imply motivation. If so, the Appellants respectfully point out that changes are suggested only with respect to oscillation frequency. Even if the statement suggested more general variations, it still would not constitute motivation to combine a PLL oscillator reference (Ito) with the charge pump of Tasdighi, for the same reason that a need for different sports car tires does not motivate a designer to select at random from a catalog of truck tires. In failing to provide any reason that a skilled person would select an oscillator from Ito for a charge pump, the Examiner has failed as the district court did in another case: "In concluding that obviousness was established by the teachings in various pairs of references, the district court lost sight of the principle that there must have been something present in those teachings to suggest to one skilled in the art that the claimed invention before the court would have been obvious." (Cites omitted) *W.L.Gore, id.*, endnote 6, at 1551, emphasis added.

Tasdighi suggests that one should use oscillators that a skilled person would deem suitable for a charge pump. Tasdighi explicitly states (col. 4 lines 39-41, part of quote set forth above): "One skilled in the art would understand the numerous varieties of oscillators which may be used in this invention." The "art" is that of charge pumps (DC to DC converters; see Field of the Invention). Thus, Tasdighi effectively directs the reader to charge pump prior art for oscillator alternatives.

Thus, the Examiner suggests no motivation for combining ring oscillator of Ito with the charge pump of Tasdighi. Tasdighi suggests no motivation for the combination, and Ito does not mention charge pumps whatsoever. It is well established that motivation for a proposed combination is required to establish *prima facie* obviousness over such combination. "Thus, every element of a claimed invention may often be found in the prior art. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific

combination that was made by the applicant." (Cites omitted) *In re Kotzab*, 217F3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)[16]. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." *In re Mills*, *id.*, endnote 12 at 682 (1432). The Examiner's failure to indicate motivation to combine Ito with Tasdighi is thus contrary to the basic patent law noted above.

In view of the foregoing, it is respectfully submitted that each of the grounds of rejection set forth by the Examiner based on combining Ito with Tasdighi fail immediately due to a lack of motivation to combine the references in the manner suggested by the Examiner. There is ample teaching of oscillators that are relevant to charge pumps, and hence no need, and no motivation, for a skilled person to modify a charge pump using oscillator designs found in non-charge pump art.

Moreover, there is reason that the skilled person would not use general purpose oscillators in charge pump designs, particularly to the extent that their output is not rectangular or nearly rectangular. All of the output waveforms of the prior art charge pumps of record are either rectangular or nearly rectangular (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). General purpose oscillators often have different waveforms. Indeed, substantially sinusoidal waveforms are quite common amongst general purpose oscillators, but have been avoided by skilled persons designing charge pumps. This negative evidence must be considered (*see W.L.Gore*, *id.*, endnote 6), and, particularly because there is no positive evidence of motivation, requires a conclusion that motivation is absent. For this lack of motivation alone, the Examiner fails to provide evidence sufficient to establish *prima facie* obviousness for any of the Appellants' claims.

Each of the Examiner's specific claim rejections over Tasdighi in view of Ito additionally fail for lack of disclosure of all claimed elements, as is demonstrated in the remarks set forth below with respect to each claim.

VII.B.3.a Rejection of Independent Claim 1 over Tasdighi in view of Ito

The Examiner's rationale in support of this ground of rejection extends from page 27 line 9 to page 28 line 7 of the Final Rejection. In it, the Examiner acknowledges that Tasdighi fails to disclose any of the clock details required by Claim 1 (c). He continues at page 27 line 17:

> However, Tasdighi does disclose the clock output of the oscillator can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from [*sic*] of oscillator" (i.e. see column 5, lines 21-22).

Tasdighi col. 4 lines 47-55 exclusively addresses changes for varying frequency, which are not relevant to any element of Claim 1.

The Appellants acknowledge that ring oscillators are commonly used in charge pumps, including various forms of current-starved ring oscillators. Thus, the form of the oscillator is not at issue. The fact that a ring oscillator may be used is not the same as saying that any ring oscillator may be used.

The reference (Tasdighi) must be considered in its entirety, including any teaching away from the asserted combination in either the reference or other prior art (*W.L.Gore, id.*, endnote 6). Considered in its entirety, Tasdighi fairly directs the reader to those of skill in the art to determine what oscillators would be suitable (Tasdighi, col. 4 lines 39-41). It is respectfully submitted that none of the charge pump prior art of record suggests an oscillator as required by Claim 1 (see generally *VII.B.2 Rejection of Claims under 35 USC § 103(a) over Tasdighi in view of Hara* for detailed support for that assertion). Certainly the Examiner has not identified any such disclosure.

Claim 1 is very specific to charge pumps. Claim 1, as presently pending, recites in part (underlining added for emphasis):

> Charge pump apparatus for generating an output voltage supply within a circuit, comprising: ... c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches ...

The underlined text of the portions of Claim 1 set forth above underscore that Claim 1 is exclusively directed to a clock for a charge pump, for controlling switching circuitry in a charge pump.

Ito is not charge pump prior art. Ito is directed exclusively to voltage controlled oscillators. The Examiner provides no reason for the desirability of taking an oscillator from a different area of art for use with a charge pump, when there is every reason to believe that charge pumps of the prior art tolerate only a very narrow range of acceptable output waveforms (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). Thus, the prior art does not suggest that it is a good idea to combine any non-charge pump oscillator with a charge pump, nor does Tasdighi, nor does Ito. The absence of such motivation immediately causes the Examiner's rationale to fail to support *prima facie* obviousness of Claim 1. But there is, additionally, evidence that the claimed combination of elements, asserted by the Examiner from bits and pieces of remotely related art using the Appellants' claim as a matrix, is indicated in the prior art to be unsuitable for charge pumps.

The foregoing circumstances are particularly analogous to those before the Federal Circuit in *W.L.Gore, id.*, endnote 6. There, as here, reason to combine the cited references was lacking; moreover, as here, the prior art contained negative teaching that tended to indicate that the asserted combination of features was undesirable. *W.L.Gore, id.*, endnote 6. In the present case, the teaching away from the asserted combination is particularly strong, because it is provided by a charge pump reference that deals extensively with current-starved ring oscillators. Hara teaches expressly that such oscillators should have five or more inverter stages (Hara, col. 5 lines 60-62). This line of argument has been set forth in greater detail in subsection *VII.B.1.a Rejection of Independent Claim 1 over Tasdighi in view of Yamauchi.*

For all of the reasons set forth above, Tasdighi in combination with Ito fails to establish *prima facie* obviousness of Claim 1. As such, Claim 1 is nonobvious over this combination, as are all of the claims depending therefrom. Therefore, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

VII.B.3.b Rejection of Claims 2-10 over Tasdighi in view of Ito

Claim 9 may stand or fall with Claim 1. The following claims are also nonobvious over Tasdighi in view of Ito for the reasons set forth above in support of the nonobviousness of Claim 1. However, they do not stand or fall with Claim 1, but are further nonobvious for at least the additional reasons set forth below.

Claim 2: Claim 2, as presently pending, recites: "The apparatus of Claim 1, wherein the plurality of transfer capacitor coupling switches are under control of the particular charge pump clock output." The switches are introduced in clause (b) of Claim 1, which recites: "a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output;" and the particular charge pump clock output is introduced in clause (c) of Claim 1.

It is respectfully submitted that Tasdighi fails to teach or fairly suggest the limitation recited in Claim 2. As noted above with respect to the rejection of Claim 18 as anticipated by Tasdighi, Tasdighi provides only a simple arrow that points between the oscillator and switching blocks to suggest some type of coupling. The arrow contains no electrical information. Furthermore, the missing descriptive matter is not inherently present, because many alternatives are possible, and indeed probable. Ito makes no suggestion whatsoever in respect to charge pumps. Accordingly, the combination of Tasdighi and Ito fail to disclose all of the limitations of Claim 2. Thus, for this additional reason, Tasdighi in combination with Yamauchi fails to establish even *prima facie* obviousness of Claim 2. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 2.

Claim 3: Claim 3 includes all of the limitations of Claim 2, with the further limitation that the clock signal be coupled "without increasing a rate of voltage rise or fall of the signal." Tasdighi discloses only an arrow (Fig. 2) to indicate some type of coupling of the clock to the charge pump switches. The arrow is not an electrical symbol, and conveys no detail whatsoever about such coupling. Ito discloses nothing whatsoever in regard to charge pumps, and thus cannot remedy the failure of Tasdighi in these regards. Thus, Claim 3 is nonobvious over Tasdighi in view of Ito for this additional reason, and the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 4: Claim 4 requires a coupling circuit coupling the clock signal "without increasing a rate of voltage rise or fall of the signal." Tasdighi completely fails to disclose this limitation. As noted above, Appellants respectfully submit that the Examiner is incorrect as a matter of law to adduce explicit limitations based on an absence of details in the reference (see, *e.g.*, *Richardson*, *id.*,

endnote 2). Ito has no charge-pump relevant disclosure to remedy the missing descriptive matter of Tasdighi. Consequently, Claim 4 is nonobvious over Tasdighi in view of Ito for this further reason. The panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 5: Claim 5 requires "a capacitive coupling circuit configured to couple one of the at least one charge pump clock outputs to a control node of one of the plurality of transfer capacitor coupling switches." Tasdighi discloses no such detail of coupling, and Ito provides no disclosure relevant to such charge-pump coupling that could remedy this missing descriptive matter. The Examiner offers the conclusory statement that "[I]t would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Ito's clock output CLKO and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering claims 5-6 obvious." The Examiner further asserts that capacitive coupling circuits "would provide one means for DC blocking to minimize possible transitioning errors." The Examiner's conjecture, which is contrary to the evidence of the prior art, cannot support a finding of *prima facie* obviousness under review. The absence of evidence provided by the Examiner does not satisfy the standard of review applied to findings of fact under the Administrative Procedure Act, which is "substantial evidence." See *In re Gartside*, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000)[17]. Claim 5 is accordingly nonobvious over Tasdighi in view of Ito for this further reason.

Claim 6: Claim 6 includes the limitations of Claim 2, above, and further requires: "corresponding capacitive coupling circuits to couple a control node of each of the plurality of transfer capacitor coupling switches to the particular charge pump clock output." Thus, Claim 6 is additionally nonobvious over Tasdighi in view of Ito for the reasons set forth above with respect to Claim 2. The additional limitations of Claim 6 are related to those of Claim 5, such that the reasoning set forth above in support of the nonobviousness of Claim 5 applies as well to Claim 6. Tasdighi fails to disclose the recited limitations, and Ito can offer no remedy in regard to charge pump coupling for the missing descriptive material in Tasdighi. As noted above, in supporting this rejection the Examiner offers conjecture instead of evidence. Therefore, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 7: Claim 7 depends from Claim 6, and thus is nonobvious over Tasdighi in view of Ito for all of the reasons that apply to Claim 6. Moreover, Claim 7 requires that: "none of corresponding capacitive coupling circuits is configured to conduct substantial charge to the transfer capacitor." As noted elsewhere, this limitation avoids an entire family of charge pumps. Tasdighi has no detail of a coupling circuit, let alone of this specific additional limitation, and thus does not support *prima facie* obviousness of Claim 7. Nor does Ito remedy this failure, for the reasons set forth above in this section. Claim 7 is thus nonobvious over Tasdighi in view of Ito for this yet further reasons, so the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 8: Claim 8 is nonobvious for all of the reasons that apply to Claim 5, as set forth in this section above. Moreover, similarly to Claim 7, Claim 8 additionally requires that: "the capacitive coupling circuit does not conduct substantial charge to the transfer capacitor." Claim 8 is therefore additionally nonobvious over Tasdighi in view of Ito for the same reasons set forth above with respect to Claim 7. Therefore, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 10: Claim 10 further requires "coupling substantial charge into the transfer capacitor via the charge pump clock output." Tasdighi provides no disclosure of this limitation, and Ito provides no relevant disclosure that could remedy the missing descriptive matter of Tasdighi. (The Examiner misinterprets Claim 10 (which describes the misinterpretation of the term "via"), a matter addressed in more detail below in subsection "VII.C Rejections Under 35 USC § 112, Second Paragraph" set forth below). Claim 10 is accordingly nonobvious over Tasdighi in view of Ito for this additional reason, and hence the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

VII.B.3.c Rejection of Independent Claim 43 over Tasdighi in view of Ito

The reasons set forth above in support of the nonobviousness of Claim 1 over Tasdighi in view of Ito are applicable as well to Claim 43, and are incorporated here by reference. The Examiner offers no teaching or suggestion in the prior art that motivates combining the PLL oscillator of Ito with the charge pump of Tasdighi. No motivation is seen. The prior art teaches that

such an oscillator would not be used in a charge pump by one of skill in the art. Hara, which discloses the only non-square clock output in the cited references of record, describes current-starved ring oscillators for charge pumps, but expressly excludes those of less than five inverter sections. The prior art of record, overwhelmingly and without exception, teaches use of square-edged, or nearly square-edged, clock outputs in charge pumps. Such outputs are incompatible with the oscillator illustrated in Ito.

VII.B.3.d Rejection of Claims 44-48 over Tasdighi in view of Ito

Claims 44-48 include all of the limitations of Claim 43, and are nonobvious over Tasdighi in view of Ito for at least the reasons set forth above. Claim 44 may stand or fall with Claim 43.

The Examiner supports for the ground of rejection of Claims 44-48 only by reference to his previous rationales for rejecting claims 1-9 and 12-17 over Tasdighi in view of Ito, and his rationales for rejecting the claims over Tasdighi in view of Hara. The rejections over Tasdighi in view of Hara are inapposite, because Ito is not in any way comparable to Hara. For Claims 45-48, the argument below addresses the support offered by the Examiner with respect to his rejection over Tasdighi in view of Ito for Claims 13, 5, 13 + 5, and 4, respectively.

Claim 45: Claim 45 requires "coupling a capacitor to the driver output node of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node." This element is indeed shown in Fig. 12 of Ito. Such a capacitor will indeed slow down the output of the clock. This feature causes the circuit of Fig. 12 of Ito to be even more contrary to all of the charge pump prior art that is of record, thus providing additional reason to conclude that a skilled charge pump designer would not attempt to modify a charge pump in accordance with the teachings of Ito. The Examiner suggests no motivation for such a modification, and the modification is contrary to all of the charge pump prior art of record. Accordingly, Tasdighi in view of Ito fails to support *prima facie* obviousness of Claim 45 for this additional reason. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 46: Claim 46 requires "coupling the first charge pump clock output to a control node of the discharging switch and/or to a control node of a charging switch via a corresponding capacitive coupling circuit." The Examiner supports rejection of related Claim 5 with a conclusory

statement that it would be obvious to do so (Final Rejection, page 28 lines 11-16). As motivation, the Examiner states that the "capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors." However, in order to sustain the rejecting conjecture cannot serve as evidence that satisfies the APA requirement of "substantial evidence" of such limitation in the cited prior art. Nowhere do either of these references suggest capacitive signal coupling, and neither provides the least suggestion as to why a skilled person might make such a modification to known charge pump circuits. The limitation recited in Claim 46 thus renders Claim 46 nonobvious over Tasdighi in view of Ito for the additional reasons of lack of motivation to modify and lack of a required element. Therefore, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 47: Claim 47 recites a limitation like that of Claim 46, and is therefore nonobvious over Tasdighi in view of Ito for all of the reasons set forth above with respect to Claim 46. Claim 47 moreover depends from Claim 45, and thus is further nonobvious for the reasons set forth with respect to Claim 45. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection.

Claim 48: Claim 48 requires (underlining added for emphasis) "coupling the first charge pump output as a signal to a control node of the discharging switch circuit <u>via a network that is not configured to increase rates of voltage change of the signal</u>." This limitation is particularly relevant with respect to prior art such as Ito, which discloses a clock that has a waveform that is substantially slower-edged than clocks taught by charge pump prior art. Though not motivated to do so, it is arguably possible for a designer to employ such a slow-edged clock consistently with a conventional charge pump. To do so, however, the resultant slow-edged clock would need to be conditioned (by means of a circuit) in order to square the clock edges. Of course, it makes little sense to first create a slow clock, only to speed the clock back up. However, this is exactly what such a design would require in order to meet the clock requirements of prior art charge pumps. This limitation thus precludes a feature that would be expected if a clock as shown in Ito was to be incorporated into a charge pump, rendering Claim 48 yet more clearly nonobvious over Tasdighi in view of Ito. In any event, neither reference discloses the relevant coupling in the manner set forth in Claim 48.

Insufficient detail is provided by either reference to draw that conclusion. Therefore, the panel is respectfully requested to reverse the Examiner as to this ground of rejection.

VII.B.3.e Rejection of Independent Claim 12 over Tasdighi in view of Ito

The Examiner supports this rejection beginning at the last full sentence of page 28 of the Final Rejection: "Interpreting Ito's Fig. 12 charge pump clock generating circuit in a different manner, the generating circuit includes an active driver circuit 53a/53b configured to source current (via 61) to driver output node CLK0 and sink current (via 53b) from the output node, wherein the generator circuit also includes circuitry 61 for limiting the source current, and circuitry 64 for limiting the current sunk. This interpretation renders obvious Claim 12."

The Examiner again misrepresents the prior art. Ito's Fig. 12 is emphatically not a charge pump clock generating circuit. It is a voltage-controlled oscillating circuit (Ito col. 1 lines 44-45). Ito makes no mention of charge pumps, and even more certainly makes no suggestion that the circuit of Fig. 12 is useful for charge pumps. Ito's interest in this circuit is only to distinguish it from his own (*e.g.*, col. 2 line 56 to col. 3 line 10).

Moreover, the Examiner fails to even make an assertion that Tasdighi in view of Ito discloses all of the limitations required by Claim 12. The combination does not, in fact, disclose all of the required elements of Claim 12. Indeed, the element underlined below is incompatible with Tasdighi. Claim 12 recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to
>
> i)circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

Tasdighi teaches square wave or "train of pulses" clock output, which are not sine-like. The disclosure of Tasdighi that is relevant to clock details, such as output waveform, is fairly set forth below (underlining added for emphasis):

1. "An oscillator 24 operating at virtually any operating frequency, such as 15 KHz to 100 KHz, produces a train of pulses which are applied to control terminals of switching transistors SW1 and SW2." (col. 3 lines 15-18). [Note that this is the only statement in Tasdighi that expressly regards waveform].

2. "Switches SW1 and SW2 may each be a conventional CMOS inverter as shown in FIG. 3, comprising an NMOS transistor 26 and a PMOS transistor 27. As the oscillator 24 voltage applied to the gates of transistors 26 and 27 alternates between a high and low voltage, transistors 26 and 27 couple either a V_A voltage or a V_B voltage to the output of the CMOS circuit." (col. 3 lines 37-43).

3. Further to 2., switches SW1 and SW2 are consistently described only as either "open" or "closed." (col. 3 lines 20-32) This again implies that the switches are not driven by intermediate voltages. Moreover, both Tasdighi and the incorporated Bingham '774 reference simplify their circuits with mechanical switch representations, and describe the switches as either "open" or "closed." (col. 3 line 56 - col. 4 line 8). Each of these three items separately suggests that the control voltage (clock) is expected to be binary or square in order to turn the switches cleanly on or off.

4. "Oscillator 14 may use conventional techniques to generate a [*sic*] oscillating frequency across terminals 66 and 67. One skilled in the art would understand the numerous varieties of oscillators which may be used in this invention. In conventional oscillators, the frequency of oscillation can be changed by . . . It should be understood that changing any parameter of oscillator 14 to adjust the oscillator frequency is envisioned for this invention." (col. 4 lines 36-41 and lines 53-55).

Each of the four items set forth above relevant to Tasdighi's teachings on clock waveforms suggests a square (or rectangular) waveform. As to item 1, "pulse" is a sudden appearance, followed by disappearance, of a voltage, suggestive of fast rise and fall times; a train of such pulses comprise a square or rectangular waveform. Item 2 emphasizes changing between just two states: between high and low, or between V_A and V_B, which again implies a square wave. As to item 3, a square wave clock is necessary for the circuit to switch quickly, so that it can behave similarly to the mechanical switches that are used to describe circuit operation. The reference to prior art in item 4 is

also suggestive of a square wave, because the prior art overwhelmingly employs square wave clock outputs for driving clock outputs.

At most, Tasdighi suggests clock waveforms as in the prior art, which is limited to square and nearly-square clock waveforms. Tasdighi expressly suggests only square or train of pulse waveforms. Tasdighi states: "One skilled in the art would understand the numerous varieties of oscillators which may be used in this invention" (col. 4 lines 39-41) Tasdighi references charge pump oscillators known at the time Tasdighi was filed. However, as noted above, each and every charge pump clock waveform illustrated in the prior art of record is rectangular or nearly rectangular (*See* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*). Accordingly, even combining Tasdighi with all of the charge pump prior art references of record in this application would not provide disclosure of clock waveforms that are remotely close to being "substantially sine-like," as required by Claim 12.

Clock waveforms disclosed by the prior art of record are clearly not "substantially sine-like." Neither of the cited references describes a clock output in a manner that is synonymous with the term "substantially sine-like." The Examiner's contention that any waveform that alternates between low and high levels may "be considered" substantially sine-like is not only conjecture, it is extraordinarily unreasonable, requiring that well-defined English technical terms be eviscerated of all ordinary meaning. The Examiner's contention can be correct only if "substantially sine-like" has no definite meaning, but can mean any alternating waveform. As such, the Examiner's contention is fairly addressed in the subsection directed to the indefiniteness rejections, and in particular in subsection *VII.C.1.b Rejection of Claims 12, 20 and 28 as Indefinite.* The arguments and evidence of that subsection are incorporated here by reference, supporting a conclusion that persons of ordinary skill will readily understand square and nearly-square waveforms as being not "substantially sine-like."

The remarks above demonstrate that a "substantially sine-like" clock waveform is incompatible with the teaching of Tasdighi, even in view of all of the prior art of record.

As set forth above in detail, *e.g.*, in subsection *VII.B.3 Rejections under 35 USC § 103(a) over Tasdighi in view of Ito*, there is no motivation to combine Ito with Tasdighi. As set forth in

more detail in that subsection (and incorporated here by reference), the three-stage current-starved ring oscillator of Ito would not be used in a charge pump by one of skill in the art. Nonetheless, remarks are set forth below to demonstrate that this combination would not render obvious Claim 12, even assuming, *arguendo*, that Ito might be combined with Tasdighi.

Ito does not suggest a sine-like clock waveform. Even assuming, *arguendo*, that the oscillator of Ito were to be combined with a charge pump of Tasdighi by a person of skill in the art at the time of Appellants' invention, there is no suggestion in Ito that a sine-like clock output as required by Claim 12 would result, or would even be desirable. Certainly in view of the substantially square-wave clock teaching of other charge pump prior art (*see* subsection *VII.B.1.e Analysis of Clock Waveforms in Prior Art of Record*), a skilled person would desire that the clock output to be as square as possible, and would therefore avoid selecting parameters that would result in a very non-square, sine-like waveform. As such, combining Ito with Tasdighi does not remedy the Tasdighi's failure of teaching or suggesting a sine-like clock waveform. Therefore, Claims 12 is nonobvious over Tasdighi in view of Ito for this reason, in addition to the impropriety of combining Tasdighi and Ito.

Independent Claim 12 is thus nonobvious over Tasdighi in view of Ito for at least the reasons set forth above. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 12, and of Claims 13-17 that depend from Claim 12.

VII.B.3.f Rejection of Claims 13-17 over Tasdighi in view of Ito

Claims 13-17 are nonobvious over Tasdighi in view of Ito at least by virtue of properly depending from independent Claim 12. Claims 13-14 and 16-17 may stand or fall with Claim 12.

Claim 15: Claim 15 depends from Claim 12 and is thus nonobvious over Tasdighi in view of Ito for all of the reasons set forth above with respect to Claim 12. Claim 15 is further nonobvious over Tasdighi in view of Ito for the reason that both references fail to disclose the limitations recited in Claim 15. Claim 15 requires: "one or more capacitive coupling networks configured to couple one of the at least one charge pump clock outputs to a control node of an active switch." As has been noted numerous times hereinabove, Tasdighi contains no details in respect of coupling the clock to the charge pump switch, and specifically includes no teaching, disclosure or suggestion that

such coupling should be accomplished as recited in Claim 15. There are no circumstances, and certainly none asserted by the Examiner, that would justify attribution of relevant subject matter to Tasdighi by inherency, common knowledge, or official notice. Accordingly, Tasdighi cannot be properly relied upon for descriptive matter that is not set forth in "as much detail as in the claim" (*Richardson, id.*, endnote 2).

Tasdighi fails to disclose, teach or fairly suggest the limitations of Claim 15. Ito contains no suggestion whatsoever in regard to charge pump switches, and thus cannot remedy the failure of Tasdighi to disclose such element of Claim 15. Thus, Claim 15 is nonobvious over Tasdighi in view of Ito, and the panel is respectfully requested to reverse the Examiner as to this rejection of Claim 15, for this additional reason.

VII.B.3.g Rejection of Independent Claim 28 over Tasdighi in view of Ito

Claim 28 recites in part (underlining added for emphasis):

> b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions such that a voltage of the first charge pump clock output is substantially sine-like.

The underlined limitation of Claim 28 is sufficiently similar to that discussed in subsection *VII.B.3.e Rejection of Independent Claim 12 over Tasdighi in view of Ito*, set forth above, such that all of the arguments and evidence set forth in that subsection are applicable with respect to Claim 28 as well. For the sake of brevity, the entire content of that subsection is therefore incorporated here by reference. It is respectfully submitted that those arguments and evidence require a conclusion, in view of the limitations of Claim 28, that Claim 28 is nonobvious over Tasdighi in view of Ito. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 28, and also as to the rejection of Claims 29-41 depending therefrom.

VII.B.3.h Rejection of Claims 29-41 over Tasdighi in view of Ito

Claims 29-41 are nonobvious over Tasdighi in view of Ito by virtue of properly depending from independent Claim 28, which is nonobvious over that combination of references for at least the reasons set forth above. Claims 29-31, 33 and 36-40 may stand or fall with Claim 28. Claims 32,

34-35 and 41 are each further distinguished over Tasdighi in view of Ito for at least the additional reasons set forth below.

Claim 32: Claim 30 is nonobvious over Tasdighi in view of Ito by virtue of depending from Claims 31, 30, 29 and 28, and for the following additional reason. Claim 32 requires (underlining added for emphasis): "coupling the TC to a connection of the source voltage during a charging period via the charge pump clock output." Charge pump circuits covered by this claim are distinguished from the "control only" family of charge pumps. In "control only" charge pumps, the clock output does not itself couple the TC to a source or output supply, but rather provides only a control signal for switching devices that provide such coupling. Tasdighi is a "control only" charge pump, because the clock does not directly drive a TC. In any event, Tasdighi does not suggest the element recited by Claim 32. Ito provides no suggestion whatsoever in regard to charge pumps, and thus cannot remedy the deficiency of Tasdighi in this regard. As such, Tasdighi combined with Ito fails to disclose all of the elements of Claim 32 for this reason, and thus does not establish *prima facie* obviousness of Claim 32. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 32.

Claim 34: Claim 34 is nonobvious over Tasdighi in view of Ito by virtue of properly depending from Claim 28, and for the following additional reason. Claim 34 requires (underlining added for emphasis): "coupling the first charge pump clock output to a control node of a TCCS circuit via a capacitive coupling circuit." Tasdighi makes no such suggestion in respect of coupling a clock to a TCCS control node. Ito makes no suggestion whatsoever in regard to charge pumps, and thus cannot remedy the deficiency of Tasdighi in this regard. As such, the combination of references fails to disclose, teach or fairly suggest all of the limitations of Claim 34 for this additional reason, rendering Claim 34 nonobvious over this combination of references irrespective of the nonobviousness of Claim 28.

The Examiner supports the rejection of claims 18-20, 22-25, 27-41, 43-51, 53-61 and 66-67 as follows (Final Rejection, page 29 last sentence, underlining added for emphasis): "These claims are obvious variations of the numerous claims already rejected within the previous descriptions, and it is not considered necessary to keep repeating redundant type explanations." Because these

rejections are over a different combination of references, this conclusory statement does not satisfy the "substantial evidence" standard required for evidence to sustain *prima facie* obviousness of these claims. In view of the absence of evidence of all of the limitations of Claim 34, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 34.

Claim 35: Claim 35 requires "coupling the associated control node of each of the actively controlled TCCS circuits to the first charge pump clock output via a corresponding capacitive coupling circuit." Tasdighi fails to disclose, teach or fairly suggest this claim limitation. Ito has no relevant teaching whatsoever, and thus cannot remedy the deficiency of Tasdighi. Therefore, the combined references do not establish *prima facie* obviousness of Claim 35. The Examiner fails to identify any evidence supporting this ground of rejection. For at least these reasons, Claim 35 is nonobvious over Tasdighi in view of Ito, and, as such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 35.

Claim 41: Claim 41 requires (underlining added for emphasis): "coupling the TC to the source voltage or to the output supply in part <u>via a passive TCCS circuit</u>." Tasdighi teaches the use of CMOS inverters as TCCSs. Each TCCS in Tasdighi is actively controlled, and thus Tasdighi fails to suggest the limitations recited in Claim 41. In rejecting the claims for indefiniteness under 35 USC 112, the Examiner indicates that he has failed to understand this claim. This issue is addressed in a separate subsection. Because Ito provides no relevant suggestion to remedy the deficiency of Tasdighi in respect to a "passive TCCS circuit," the combination of references fails to fairly suggest all of the limitations of Claim 41. Claim 41 is accordingly nonobvious over Tasdighi in view of Ito, and the panel is respectfully requested to reverse the Examiner, at least for this additional reason.

<u>VII.B.3.i Rejection of Independent Claim 18 over Tasdighi in view of Ito</u>

Relevant limitations of Claim 18 are set forth above in subsection *VII.A.1 Rejection of Claim 18 as Anticipated by Tasdighi.* All of the arguments and evidence set forth in that subsection are relevant to this ground of rejection, and are accordingly incorporated here by reference. The underlined text of Claim 18 set forth in that subsection includes: "a <u>single-phase charge pump clock output</u> coupled <u>passively, without conveying substantial transfer current, to control nodes of each of the source switching devices</u> ... for all of the source switching devices, the charge pump clock output

further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices."

Ito teaches single-phase clocks, but is completely silent regarding charge pumps or coupling of clocks to TCCSs. As such, Ito can make no suggestion relevant to the underlined limitations that might remedy any deficiency of Tasdighi in that regard. Because Ito adds nothing to Tasdighi in this regard, this ground for rejection is entirely redundant of the rejection of Claim 18 as anticipated by Tasdighi. Accordingly, all of the arguments and evidence set forth in subsection *VII.A.1* that support the conclusion that Claim 18 is not anticipated by Tasdighi, are applicable to support a conclusion that Claim 18 is nonobvious over Tasdighi in view of Ito. Therefore all of those arguments are incorporated here by reference.

The Examiner supports his rejection of claims 18-20, 22-25, 27-41, 43-51, 53-61 and 66-67 as follows (Final Rejection, page 29 last sentence, underlining added for emphasis): "These claims are obvious variations of the numerous claims already rejected within the previous descriptions, and it is not considered necessary to keep repeating redundant type explanations." The Examiner thus offers no reason why combining Ito with Tasdighi might render Claim 18 obvious. As such, and in view of the argument set forth in subsection *VII.A.1* that Claim 18 is not anticipated by Tasdighi, it is respectfully submitted that Claim 18 is nonobvious over Tasdighi in view of Ito. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 18, and as to Claims 19-20 and 22-23 depending therefrom.

VII.B.3.j Rejection of Claims 19-20 and 22-23 over Tasdighi in view of Ito

Each of these claims is nonobvious over Tasdighi in view of Ito at least by virtue of depending from Claim 18, which is nonobvious for at least the reasons set forth above. Claims 20 and 22-23 may stand or fall with Claim 18. Claim 19 is nonobvious over the cited combination of references for further reasons, as set forth below.

Claim 19: Claim 19 requires an entire second stage of the charge pump, and further requires that "the charge pump clock output is coupled to all of the second-source switching devices ... and ... to all of the second-output switching devices ... ." As may be seen in the prior art of record, such additional stage TCCSs invariably require additional clock phases to be driven. In any event, neither

Tasdighi nor Ito teaches, discloses, or fairly suggests the limitations of Claim 19. Tasdighi illustrates a charge pump with a second stage; the charge pump is disclosed in detail in the Bingham '774 patent incorporated by reference, where it may be seen that the two-stage charge pump employs two clock phases. Thus, the evidence set forth in the cited art is contrary to the Examiner's rejection, because the two-stage charge pump of Tasdighi clearly does not have a single-phase charge pump.

The Examiner declined to provide evidence supporting this ground of rejection, relying instead on rationale set forth in previous rejections (Final Rejection, page 29 lines 14-19). Though none of the identified previous rejections are apposite, Claim 19 also stands rejected over Tasdighi in view of Yamauchi. However, Appellants respectfully submit that the rationale provided therein can fairly be characterized as unwarranted and unnecessary conjecture. The Examiner states (*see*, Final Rejection, page 19 lines 10-19, underlining added for emphasis): "However, it would have been obvious to one of ordinary skill in the art to add a second charge pump stage/apparatus to the charge pump apparatus of claim 18 .... It could have the same basic structure as Tasdighi's Fig. 2, wherein the second charge pump stage could be coupled in parallel to the charge pump apparatus, and both would receive the same charge pump clock output."

The Federal Circuit disapproves such conjecture: "That one *could* invent such a cable tie is unquestioned. Caveney *did*. The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made. *Panduit, id.*, endnote 8, at 1092. The Examiner's conjecture is thus disapproved by the Federal Circuit. Moreover, asserted "facts" supported only by conjecture, as are the Examiner's, will not be sustained by a reviewing court because they fail the "substantial evidence" threshold established by the Administrative Procedures Act (*see, e.g., Energizer v. ITC, id.*, endnote 21).

The Examiner attributes his hindsight-based circuit conjecture on Tasdighi's Fig. 2. This is particularly egregious in view of the fact that Tasdighi's Fig. 4 is an example of a dual-stage charge pump such as is described in Claim 19, and the further fact that details for the coupling of such a circuit are incorporated in Tasdighi by reference (see col. 3 lines 45-47 incorporating Bingham '774). The coupling details thus incorporated by reference are inconvenient for the Examiner, however,

because they are contrary to the limitations of Claim 19: Bingham '774 teaches the use of plural clock phases, contrary to required element (h) of Claim 19, which recites in part "the charge pump clock output is coupled to all of the second-source switching devices ... and ... to all of the second-output switching devices... ." Thus, the Examiner provides no actual evidence to support this ground of rejection, and the evidence available to him indicates that his conjecture is not only improper, but contrary to the facts.

Therefore, Tasdighi and Ito together most certainly fail to disclose the required limitations of Claim 19 for these additional reasons, and, as such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 19.

VII.B.3.k Rejection of Independent Claim 49 over Tasdighi in view of Ito

Claim 49 is a method claim defined by limitations that are, in general, similar to those recited in apparatus Claim 18. As noted above because a skilled person would not look to VCO art for charge pump oscillators in view of the particular requirements of charge pumps, there is no motivation for the combination asserted by the Examiner.

Claim 49 recites in part (underlining added for emphasis):

a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

The Examiner's rationale for this rejection is not clear, because he has declined to explicitly identify the evidence upon which he relies (see Final Rejection, page 29 last sentence). Because the Examiner refers to rationale set forth in claims "rejected within the previous descriptions," the Appellants address the evidence presented in support of the rejection of Claim 49 over Tasdighi in view of Yamauchi, which is set forth below (underlining added for emphasis):

> Since single phase charge pump clock output CLK is passively coupled (e.g. coupled by a straight line with no intervening elements) to the control nodes of the charging/discharging switches (e.g. see Tasdighi's transistors 26,27 shown in Fig. 3, with respect to SW1,SW2 shown in Fig. 2), and the gate of each MOS transistor will substantially isolate transfer capacitor (TC) C1 of Tasdighi from Yamauchi's clock output CLK, claim 49 is rendered obvious."

Ito makes no disclosure relevant to the coupling details that are primarily recited in Claim 49, as set forth above, and indeed makes no suggestion in respect of charge pumps at all. As such, this ground of rejection of Claim 49 is no more effective than a rejection of Claim 49 as anticipated by Tasdighi.

Tasdighi does not fairly suggest the limitations of Claim 49 underlined above. The Examiner's "evidence" includes an unsupported assumption that the clock output is single-phase. If Tasdighi provided coupling detail that was sufficient to show how a single-phase clock could be applied to the CMOS inverters and still provide proper drive to the inverters, such an assumption might be reasonable. However, Tasdighi provides no such detail. The Examiner's reliance on "a straight line with no intervening elements" is so blatantly incorrect as to appear disingenuous, for the "straight line" does not touch any of SW1, SW2, or 26,27, but rather is merely an arrow that shows some type of connection between the blocks. It is true there are "no intervening elements," but there is also no intervening line. One does not ordinarily place elements on a non-electrical arrow symbol. The Examiner's "evidence" is thus pure conjecture.

Moreover, the Examiner's conjectured coupling would render the circuit unsatisfactory for its intended purpose. As set forth above in detail in subsection *VII.A.1 Rejection of Claim 18 as anticipated by Tasdighi*, incorporated here by reference, coupling a single-phase clock output directly to two CMOS inverters would necessarily cause two MOSFETs to be turned on directly across the TC (shorting the TC) during each transition between high and low of the clock.

Moreover, as also set forth in detail in subsection *VII.A.1* (noted above), Tasdighi's conjecture as to the coupling that he attributes to Tasdighi is completely unsupported by the prior art of record.

Finally, Tasdighi fails to disclose the elements required by Claim 49 in the detail indicated in the Claim, as is required to support anticipation (*see, e.g., Richardson, id.*, endnote 2). While this ground of rejection is nominally obviousness over Tasdighi in view of Ito, Ito adds absolutely nothing relevant to Tasdighi in this regard, and thus cannot remedy the descriptive matter missing from Tasdighi.

In the absence of detail showing coupling sufficient to work with a single-phase clock, and in the absence of detail clearly showing that the clock is and remains single-phase, neither detail can properly be assumed. Neither detail is inherent, because alternatives are not only possible, but, in fact, common. Doctrines such as "common knowledge" are certainly inappropriate: an element certainly isn't "common knowledge" when, as here, it is contrary to the prior art, or when, as here, such element results in making the circuit unsuitable for its intended purpose. (Further support for the foregoing summary is set forth in subsection *VII.A.1.f Other Doctrines for Asserting Missing Descriptive Material are Also Unavailing.*)

For the foregoing reasons, it is respectfully submitted that Tasdighi, whether in combination with Ito or not, fails to disclose, teach or fairly suggest all the limitations of Claim 49. As such, Tasdighi in view of Ito does not sustain *prima facie* obviousness of Claim 49. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 49.

VII.B.3.l Rejection of Claims 50-51 and 53-59 over Tasdighi in view of Ito

Claims 50, 54 and 57-59 may stand or fall with Claim 49. Claims 51, 53 and 55-56 are each nonobvious over Tasdighi and Ito for additional reasons, as set forth below.

Claim 51: In addition to the limitations of Claim 49, Claim 51 incorporates the following limitations "coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output;" and "coupling the TC to a voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." These limitations constitute further detail that is absent from the disclosure of both Tasdighi and Ito, even including Bingham '774 incorporated in Tasdighi by reference. Tasdighi and Ito themselves are devoid of relevant disclosure. The coupling of a single-phase clock to a plurality of charging TCCSs and a plurality of discharging TCCSs associated with a

TC (transfer capacitor) in Bingham '774 is not only active, but it explicitly develops a plurality of different phases that are then connected to the different TCCSs. As such, the combination of Tasdighi and Ito, even further including Bingham '774, fails to disclose all of the limitations of Claim 51 for these further reasons. Tasdighi and Ito thus further fail to support *prima facie* obviousness of Claim 51, wherefore the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 51.

Claim 53: Claim 53 recites in part: "coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output." This limitation constitutes further detail that is missing from the disclosure of both Tasdighi and Ito. The coupling of a single-phase clock to a plurality of charging TCCSs associated with a TC (transfer capacitor) in Bingham '774 (incorporated by reference in Tasdighi) is not only active, but it explicitly includes developing a plurality of different phases that are then connected to the different charging TCCSs. As such, the combination of Tasdighi and Ito, even further including Bingham '774 (incorporated by reference in Tasdighi), fails to disclose all of the limitations of Claim 53 for this further reason. Tasdighi and Ito thus fail to support *prima facie* obviousness of Claim 53. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 53.

Claim 55: Claim 55 includes the limitations of Claim 54 as well as Claim 49 by virtue of dependency, and further requires "coupling the charge pump clock output to a control node of each TC charging switch, and to a control node of each TC discharging switch, via corresponding capacitive coupling circuits." Neither Tasdighi nor Ito discloses this limitation, and the combination thus fails to support *prima facie* obviousness of Claim 55 for this additional reason. The Examiner has declined to specifically identify support for this ground of rejection (see Final Rejection page 29, lines 14-19). Because each rationale for rejecting other claims having been addressed with respect to such other rejected claims, there is no new rationale set forth in rejecting Claim 55 for the Appellants to consider and address. However, it is noted that the relevant prior art of record, despite the Examiner's presumably conscientious search for the missing descriptive matter, contains not a single instance in which the clock in a "bridge" or "control only" charge pump, such as is used in Tasdighi, is capacitively coupled to its TCCSs (see the analysis of prior art set forth above in regard to Claim 46 in subsection *VII.B.2.d Rejection of Claims 44-48 over Tasdighi in view of Hara*). This

constitutes substantial evidence that one of skill in the charge pump arts would not modify the Tasdighi charge pump as suggested by the Examiner. As noted above, integrated circuit designers do not insert capacitors in their designs just because it can be done. Capacitors consume substantial integrated circuit area and introduce problems with establishing bias. As such, the skilled person would employ active coupling techniques, which are more flexible and consume less chip real estate. The Examiner suggests no motivation for such a modification, and the evidence supports a conclusion that such modification is undesirable.

Thus, neither Tasdighi nor Ito discloses the required limitations. Even if the limitations were present in one of the references, there is absolutely no motivation for combining the references as suggested by the Examiner and thereby modifying the charge pump described in Tasdighi. Tasdighi and Ito, in combination, thus fail to sustain *prima facie* obviousness of Claim 55 for these substantial additional reasons. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 55.

Claim 56: Claim 56 is similar to Claim 55, except that it does not depend from Claim 54. With that exception, all of the arguments for further nonobviousness of Claim 55 over Tasdighi in view of Ito are applicable to support the further nonobviousness of Claim 56 over that combination of references. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 56 for the reasons set forth above with respect to Claim 55.

VII.B.3.m Rejection of Independent Claim 24 over Tasdighi in view of Ito

Claim 24 recites in part (underlining added for emphasis):

a) a transfer capacitor for conveying charge from a voltage source to the output voltage supply;

b) one or more source switching devices disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;

c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source; and

d) a capacitive coupling circuit coupling a charge pump clock output to one of the control nodes corresponding to a source switching device or to an output switching device.

The Examiner fails to provide explicit evidence to support this ground of rejection. While the Examiner declines to offer evidence supporting the rejection of Claim 24 over Tasdighi in view of Ito, he refers to rejections related to the "Tasdighi/Hara" references. (see p. 29 of Final Office Action, lines 14-19) Thus, reference is made to Appellants' argument set forth above in subsection *VII.B.2.l Rejection of Independent Claim 24 over Tasdighi in view of Hara*, the entire content of which is incorporated here by reference, and which is applicable *mutatis mutandis*. This ground of rejection is even less meritorious, however, because Ito contributes even less than Hara in providing descriptive material admittedly missing from Tasdighi. Hara is at least relevant to charge pumps, while no motivation is seen for combining Ito with charge pump prior art such as Tasdighi. As noted above, a skilled person (at the time of the Appellants' invention) would understand that charge pump oscillators have special requirements, and would accordingly look to the numerous available charge pump prior art references for a suitable oscillator, rather than to PLL/VCO prior art such as Ito. Moreover, Hara at least discloses a capacitor used for coupling a signal. While said capacitor is not actually relevant to coupling clocks to charge pump switches (TCCSs), it is at least a colorable attempt to find evidence of the existence of the elements required by Claim 24. Ito shows no such capacitive coupling, and, in fact, contributes nothing whatsoever to this rejection. The Examiner has acknowledged that Tasdighi fails to disclose capacitive coupling (see, page 22 lines 16-20 of the Final Rejection). Furthermore, the Examiner has expressly declined to indicate evidence that Tasdighi and Ito together disclose all of the elements of Claim 24.

Admitting Tasdighi's omitted descriptive material, without pointing to such material in Ito, the Examiner effectively admits that the combination of Tasdighi and Ito together fail to disclose all of the elements required by Claim 24. Admission or not, Tasdighi and Ito together clearly do fail to disclose all the required elements, and thus fail to establish *prima facie* obviousness of Claim 24 or any claim depending therefrom. The argument set forth in subsection *VII.B.2 Rejections under 35 USC § 103(a) over Tasdighi in view of Hara* provide further reasons to conclude that Claim 24, and all claims depending therefrom, is nonobvious over this combination of references. Accordingly, the

panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 24-25 and 27.

VII.B.3.n Rejection of Claims 25 and 27 over Tasdighi in view of Ito

Claims 25 and 27 are each nonobvious over Tasdighi in view of Ito for the reasons set forth above, by virtue of depending from independent Claim 24. Each is also nonobvious for further reasons, as set forth below.

Claim 25: Claim 25 requires "a second capacitive coupling circuit coupling the charge pump clock output to an output switching device control node." Neither of the cited references discloses, teach or fairly suggest this additional limitation, and thus fail to establish *prima facie* obviousness of Claim 25 for this additional reason. The Examiner declines to provide evidence to support this ground of rejection (see Final Rejection, page 25 lines 11-13). The rationale the Examiner presumably intended to reference is demonstrated, in the immediately preceding subsection, to be inadequate to sustain this ground of rejection. In the absence of new rationale, it is respectfully submitted that this ground of rejection is not properly supported. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 25.

Claim 27: Claim 27 depends from Claim 25, and is therefore nonobvious over the cited references for all of the reasons set forth above for Claims 24 and 25. Claim 27 further requires that "all source switching devices disposed in series between the transfer capacitor and the voltage source, and all output switching devices disposed in series between the transfer capacitor and the output voltage, are capacitively coupled to the charge pump clock output." This further coupling detail is not disclosed in either of the cited references, thus precluding *prima facie* obviousness of Claim 27 for this additional reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 27.

VII.B.3.o Rejection of Independent Claim 60 over Tasdighi in view of Ito

Claim 60 is a method claim having many similarities to Claim 24, discussed hereinabove. The arguments and evidence set forth above in subsections *VII.B.2.l Rejection of Independent Claim 24 over Tasdighi in view of Hara* and *VII.B.3.m Rejection of Claim 24 over Tasdighi in view of Ito*

are incorporated here by reference. Due to the similarities between Claim 60 and Claim 24, those subsections are relevant *mutatis mutandis* to support a conclusion that Claim 60 is nonobvious over Tasdighi in view of Ito.

Claim 60 requires (underlining added for emphasis):

> a) coupling a first charge pump clock output to a control node of a TC charging switch via a first capacitive coupling network that does not conduct a significant portion of the charge for the output;
> b) coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output;
> c) coupling a second charge pump clock output to a control node of a TC discharging switch via a second capacitive coupling network that does not conduct a significant portion of the charge for the output; and
> d) coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output.

Claim 60, though worded substantially differently than Claim 24, nonetheless is nonobvious over Tasdighi in view of Ito for much the same reasons as is Claim 24. The Examiner declines to offer evidence to support this ground of rejection because it is redundant (see Final Rejection, page 29 last sentence). Neither Tasdighi nor Ito suggests any capacitive coupling as required by Claim 60, let alone the two distinct capacitive coupling networks required in Claim 60. The Examiner admits as much by admitting that such descriptive material is missing from Tasdighi (see page 22 lines 14-20 of the Final Rejection), and by failing to suggest another source for such missing descriptive material. This combination of references fails to teach, disclose or fairly suggest all of the limitations required by Claim 60, and as such fails to establish *prima facie* obviousness of Claim 60. Given that Ito contributes nothing whatsoever to support this ground of rejection, it is rather moot that no motivation exists to combine Ito with Tasdighi.

The above remarks, in addition to those from other subsections as noted above, amply support a conclusion that Claim 60 is nonobvious over Tasdighi in view of Ito. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 60, and as to all claims depending therefrom.

VII.B.3.p Rejection of Claims 61 and 66-67 over Tasdighi in view of Ito

Each of these claims is nonobvious over the cited references by virtue of depending from independent Claim 60, and for the following additional reasons.

Claim 61: Claim 61 requires that "the second charge pump clock output is the first charge pump clock output." Neither Tasdighi nor Ito teaches coupling a charge pump clock to TCCSs at a level of detail that permits this requirement to be fairly assumed. Prior art charge pumps, as evidenced by the prior art references of record, always use different clock signals to control the different TCCSs. There is no reason to think that they would not continue to use different clock signals, even if (for some reason) they employed capacitive coupling. The only truly relevant details in either of these references are incorporated in Tasdighi by reference to Bingham '774, which teaches use of plural clock signals, thus contradicting the Examiner's contention. Because this limitation cannot fairly be said to be taught or disclosed by either Tasdighi or Ito, Claim 61 is rendered nonobvious over that combination of references for this additional reason.

Claim 66: Claim 66 depends from Claim 60, and further requires (underlining added for emphasis and clarity) "capacitively coupling a control node of each actively controllable TC coupling switch that is incorporated within a charge pump to a corresponding charge pump clock output." Neither Tasdighi nor Ito fairly suggests even one such capacitive coupling circuit. Far less does either reference teach, disclose or fairly suggest such uniform use of capacitive coupling circuits. Accordingly, Tasdighi combined with Ito fails to establish *prima facie* obviousness of Claim 66 for this additional reason. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 66 for this additional reason.

Claim 67: Claim 67 is nonobvious over the cited references by virtue of depending from Claim 66, and further requires that "all of the corresponding charge pump clock outputs are a common single-phase output." As noted above with respect to the rejection of Claim 61, the prior art invariably employs multiple clock phases for controlling TCCSs in control-only charge pumps such as Tasdighi's. Bingham'774, incorporated by reference in Tasdighi, teaches plural clock phases for control. Neither Ito nor Tasdighi teach or suggest anything to the contrary, nor is there any other reason that a skilled person would couple a single-phase clock to all of the TCCSs. Due to the

failure of both Tasdighi and Ito to disclose, teach or fairly suggest this additional limitation, that combination of references fails to sustain *prima facie* obviousness of Claim 67 for this additional reason. As such, the panel is respectfully requested to reverse the Examiner as to this rejection of Claim 67.

VII.C Rejections Under 35 USC § 112, Second Paragraph

Interpretation of the definiteness requirement of 35 USC § 112, Second Paragraph, has gradually become more lenient toward claim drafting imperfections. The test has long been whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081 (Fed. Cir. 1986)[18]. Recent interpretation by the Federal Circuit is even more forgiving: "When a claim is not insolubly ambiguous, it is not invalid for indefiniteness." *Marley Mouldings, Ltd., v. Mikron Indus.*, 417 F.3d 1356, 1361, 75 U.S.P.Q.2D 1954 (Fed. Cir. 2005)[19], citing *Bancorp Servs., L.L.C. v. Hartford Life Ins. Co.*, 359 F.3d 1367, 69 USPQ2d 1996 (Fed .Cir. 2004)[20].

In the Amendment After Final Rejection submitted by the Appellants on October 11, 2005, the Appellants proposed amendments to Claims 13, 43, 46-48, 60 and 62 in view of the Examiner's rejection of these claims as indefinite. The proposed amendments would enhance clarity of the claims, but neither the proposed amendments, nor the failure to address these claims hereinbelow, is an admission that the claims, as presently pending, are "insolubly ambiguous" so as to fail to comport with the definiteness requirements of 35 USC § 112, Second Paragraph. Those claims are proposed for allowance, possibly contingent on the entry of certain amendments to enhance clarity.

VII.C.1 Rejection of Selected Claims as Indefinite

Claims 10, 12, 14-15, 19-21, 27-28, 34-36, 39, 41-42, 45, 50-53, 56, 63 and 65-66 stand rejected as indefinite, but it is respectfully submitted that none of these will benefit from amendment. The remarks below therefore demonstrate that each of these claims satisfies the requirement of definiteness.

"Insolubly ambiguous" is the high threshold which, as noted above, is required to render claim language indefinite. The remarks below briefly describe why one of ordinary skill in the

charge pump art would understand what is covered by each of the enumerated claims, as presently pending. The remarks demonstrate that each claim satisfies the standard for definiteness as enunciated, for example, in *Orthokinetics,* (*id.*, endnote 18). The remarks also amply support a conclusion that each claim is far from "insolubly ambiguous," and thus far from indefinite under 35 USC § 112, Second Paragraph (*Marley*, *id.*, endnote 19).

An effort has been made to group these claims logically in accordance with the nature of the Examiner's stated grounds for the rejections.

VII.C.1.a Rejection of Claim 10 as Indefinite

The Examiner states (Final Rejection, page 7 beginning line 16, underlining and italics added for emphasis and reference): "[T]he phrase 'coupling substantial charge into the transfer capacitor via the charge pump clock output' in claim 10 needs clarification." For example, does the phrasing imply the coupled charge actually comes from the clock output, or is the amount of coupled charge only *controlled* by the clock output?" In response to the Examiner's query, it is respectfully submitted that said phrasing does not merely imply the underlined meaning, it requires that meaning explicitly. This would be readily understood by one of skill in the art, exercising care in parsing the language, because "via" is a well understood word whose preferred meaning is "by a route that touches or passes through; by way of." ("via" definition 1., Webster's Encyclopedic Unabridged Dictionary of the English Language, Dilithium Press, Ltd. 1989). Furthermore, Claim 1 recites "under control of at least one charge pump clock output. Thus, clearly if the claim was intended to convey merely "under control of" a clock, it would so state explicitly.

A less equivocal statement cannot be accurately made, because there is always a finite amount of charge transferred "via the clock output" via parasitic capacitances or other leakage routes. In several embodiments (see, *e.g.*, Claim 12(b)), substantial charge transfer via the charge pump clock output is explicitly precluded, in order to clearly distinguish that family of charge pumps ("direct drive") wherein the "clock" is also the primary source of current to the transfer capacitor. In other embodiments, such as Claim 1, such transfer of current via the charge pump clock output is not precluded, and Claim 10 serves to explicitly cover charge pumps of that family. Thus, due to the existence of a family of charge pump circuits that conduct substantial current to the transfer

capacitor via the clock output (*see* subsection *V.C Single-Phase Clock Coupled Passively without Transfer Current to Each TCCS* for elaboration), such terminology is needed to distinguish whether or not a particular claim encompasses, or indeed is limited to, the "direct drive" family of charge pumps.

In view of the foregoing remarks, it is respectfully submitted that the skilled person would readily understand the challenged language "coupling substantial charge into the transfer capacitor via the charge pump clock output," and that such language is far from being "insolubly ambiguous." As such, rejection of Claim 10 as indefinite is improper. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 10.

VII.C.1.b Rejection of Claims 12, 20 and 28 as Indefinite

The Examiner notes an ambiguity between Claims 12 and 15, which is acknowledged and believed will be resolved by entry of the proposed amendment of Claim 15 as set forth in the Amendment After Final Rejection submitted by the Appellants on October 11, 2005.

Substantially Sine-Like: To support his rejection of Claims 12, 20 and 28 as indefinite, the Examiner states (Final Rejection, beginning at page 7 last full sentence, emphasis in original): "It is not clear what "substantially sine-like" means in each of claims 12, 20, and 28. Therefore, clarification is requested that clearly explains what this "sine-like" limitation actually means. For example, the original disclosure only mentions the output voltage "may oscillate substantially rail-to-rail ... and may have a significantly sine-like shape" on the last lines of paragraph 050 (see page 12). However, there is no figure, or any other original description, which clearly shows or defines what may be considered "sine-like." Therefore, if a clock generating circuit provides an output that does not have fast (or sharp) rise and fall times when alternately transitioning between high and low levels, couldn't this type of output be considered "sine-like"? Also, it is well known that a ring oscillator is basically an analog circuit, and thus its output would be "sine-like.""

In response to the Examiner's inquiries, the output he describes would be "sine-like" if the waveform was significantly like a sine wave. As set form in more detail below, the term "sine-like" is far more precisely defined, and thus limited in scope, than is the Examiner's proffered definition ("an (oscillating) output that does not have fast rise and fall times") because a sine waveform itself is

so precisely known. "[A]n output that does not have fast (or sharp) rise and fall times when alternately transitioning between high and low levels" could certainly not, without much more, be considered "sine-like;" but even if it could, the Examiner has shown no example whatsoever of a waveform such as he himself describes.

It is respectfully submitted that the Examiner's assertion that a ring oscillator is basically an analog circuit, and thus would have a "sine-like" output, is unsupported by any evidence of record, and is illogical because it leads to an absurd conclusion. The record clearly lacks any rationale or evidence whatsoever to support the Examiner's assertion. Moreover, the assertion leads to an absurdity, as follows: Because, at some level, all circuits are "basically analog," the Examiner's assertion requires an absurd conclusion that the output of all circuits is "sine-like." Thus, the Examiner's assertion is unsupported and illogical, and cannot reasonably support a rejection of a claim as indefinite.

A figure or illustration of a sine wave is unnecessary to persons of skill in the relevant art, because the definition is precise, available to all, and extremely well known to all those of skill in the relevant art, being fundamental to the entire field of electrical engineering.

All claims rely upon English words that do not have mathematically precise definitions. A mathematical function is so precise that it is extremely narrow, generally much narrower in literal scope than even extremely detailed descriptions in non-mathematical English. The recited limitation "substantially sine-like" merely ensures literal coverage of imprecise waveforms. The term "substantially" is frequently used thus to broaden an otherwise razor-thin mathematical definition.

The present circumstances compare very favorably to those in *Andrew Corp. v. Gabriel Electronics, id.*, endnote 11. There, the claims contained numerous imprecise quantities: "The district court held the Knop patent claims invalid, stating that terms in the claims such as "approach each other", "close to", "substantially equal", and "closely approximate", with reference to the E-plane and H-plane RPEs, were too vague to satisfy the requirement of definiteness stated in 35 U.S.C. § 112." The court, however, disagreed, stating: "The criticized words are ubiquitous in patent claims. Such usages, when serving reasonably to describe the claimed subject matter to those of skill in the field of the invention, and to distinguish the claimed subject matter from the prior art,

have been accepted in patent examination and upheld by the courts." *Andrew, id.*, endnote 11, at 821. Indeed, the court in *Andrew* quoted from a previous opinion to underscore the impropriety of requiring excessive precision: "to accept Beckman's contention [that the term "close proximity" is indefinite] would turn the construction of a patent into a mere semantic quibble that serves no useful purpose." *Andrew, id.*, endnote 11, at 821 [citing *Rosemount, Inc. v. Beckman Instruments, Inc.*, 727 F.2d 1540, 1546-47, 221 USPQ 1, 7 (Fed. Cir. 1984)].

It is acknowledged that the present limitation "substantially sine-like" is imprecise, because it does not require the waveform to be a sine wave. In *Andrew*, the claim limitation "which produces substantially equal E and H plane illumination patterns" (*Andrew, id.*, endnote 11, at 821) is analogous, and at least equally imprecise. In both situations, the unqualified description would require mathematical precision (the terms "equal" in *Andrew*, and "sine" wave presently, both have precise and well-known mathematical meanings). In both situations, a requirement for such mathematical precision is avoided by the term "substantially." In both situations, the comparison is of a pattern (a waveform, presently, and illumination patterns in *Andrew*). As such, the conclusion of the court in *Andrew* applies perfectly to the present facts to preclude a finding that the limitation "substantially sine-like" is indefinite.

Those of ordinary skill in the electronic circuit design arts are extremely familiar with the mathematical function that defines a sine waveform, because the sine function is central to much of electrical engineering. A sine waveform is mathematically defined, as is the relationship "equal to." "Substantially sine-like" is equally as clear as "substantially equal." The fact that "substantially" extends the range of covered waveforms beyond the precise mathematical construct "sine" will be reasonably clear to those of skill in the art.

"We have held that a claim is not indefinite merely because it poses a difficult issue of claim construction; if the claim is subject to construction, i.e., it is not insolubly ambiguous, it is not invalid for indefiniteness." *Bancorp Services, id.*, endnote *20*, citation omitted. It is respectfully submitted that "substantially sine-like" is readily understood by one of skill in the art, and is far from being "insolubly ambiguous." The challenged limitation of Claim 12 is thus easily the sort of claim

language that the Federal Circuit has determined, in numerous decisions involving different facts, to be not indefinite.

In view of the remarks, evidence and law set forth above, it is respectfully submitted that a "substantially sine-like" waveform is well defined in a manner that would be readily understood by those familiar with the sine shape, *i.e.*, all those of at least ordinary skill in the electronic arts relevant to charge pumps. This language is very far from meeting the "insolubly ambiguous" threshold required to sustain a rejection as indefinite. Accordingly, this ground of rejection of Claims 12, 20 and 28 is unwarranted, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claims 12, 20 and 28.

VII.C.1.c Rejection of Claim 14 as Indefinite

The Examiner states (Final Rejection, page 8 lines 8-11): "It is not understood how the 'circuitry to limit the current source capacity' and 'circuitry to limit the current sink capacity' in claim 14 relates to claim 12's circuitry that limits source current and current sunk." The answer is simple: the clock generating circuit of Claim 12 requires only "an active driver circuit," and the current limits apply to limit the current provided by "the driver circuit." Claim 14, however, further requires (underlining for emphasis) "a plurality of active driver circuits," and, as stated, the current limits apply to "each of the active driver circuits." This should be abundantly clear upon careful consideration, and certainly is not "insolubly ambiguous."

VII.C.1.d Rejection of Claim 15 as Indefinite

The Examiner supports this ground of rejection of Claim 15 as follows: "It is not clear how claim 15's "an active switch" relates to the "plurality of active switches" recited on line 4 of claim 12. For example, is the switch of claim 15 one of the switches of claim 12, or can it be referring to some other active switch?"

Claim 15 is reasonably clear. Given that an indefinite article was used in Claim 15, the "active switch" in Claim 15 need not be one of those referred to in Claim 12. Claim 15 is thus clearly not "insolubly ambiguous" so as to violate the requirements of 35 USC 112, second paragraph. Nonetheless, upon consideration, a slight amendment of this claim would be preferred,

and would render the claim easier to parse, if not more definite. It is therefore respectfully proposed that the panel deem Claim 15 allowable contingent on amending it by replacing "an active switch" by --at least one of the plurality of active switches--."

VII.C.1.e Rejection of Claims 19, 21 and 27 as Indefinite

The Examiner states (Final Rejection, page 8 lines 13-14, emphasis in the original): "The use of 'a second charge pump stage' in the preamble of claim 19 implies a first stage that has not been clearly identified within the claim's chain of dependency."

The Examiner continues (Final Rejection, page 8 lines 14-18, emphasis in the original): "It is not clear in claim 19 how 'all of the second-source switching devices' (line 7) and 'all of the second-output switching devices' (line 9) relate to the switching devices recited on lines 3 and 5 if there is only one of each. For example, does the use of 'all' refer to at least two, or was 'all' meant to be --each--?" The Examiner's inquiry is readily addressed, and no substitution of words is necessary or desirable to clarify any of Claims 19, 21 and 27.

It is common knowledge that "all" of a quantity of items is the total number of such items, regardless of whether the total number is 0, 1, many, or an undifferentiated mass. Dictionaries do not address a range for the word, but actual usage is clear. For example, a popular aphorism states "Half of something is better than all of nothing," precisely because "all of nothing" is nothing. If "all" can mean "zero" or "two," it can certainly mean "one" in the appropriate circumstances. Accordingly, the term "all", as used in Claims 19, 21 and 27 is correct and unambiguous.

The Examiner's statements in support of his rejections of Claims 21 and 27 as indefinite is essentially the same as set forth above with respect to Claim 19, and are addressed by the remarks above defining "all" as used in those claims. The Examiner further asks whether --each of the-- was meant instead of "all." The answer is no: the language in each of Claims 19, 21 and 27 is correct as presently pending. It is respectfully submitted that the language of Claims 19, 21 and 27, far from being "insolubly ambiguous" and therefore indefinite, to the contrary is eminently clear and precise. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claims 19, 21 and 27.

VII.C.1.f Rejection of Claim 34 as Indefinite

The Examiner states (Final Rejection, page 9 lines 4-7): "It is not understood how the single 'a TCCS circuit' of claim 34 relates to 'a TC-coupling switch ("TCCS") circuit' (lines 3-4), or to 'a discharging TCCS circuit' (line 6), both recited within claim 28."

The recitation: [a TC-coupling switch ("TCCS") circuit] is definitional, indicating that TCCS represents TC coupling switch. TC itself is an acronym for "transfer capacitor," so TCCS means (and in fact is an acronym for) "transfer capacitor coupling switch." A switch may refer to a single device, while a "circuit" more gracefully suggests (though it does not require) that a plurality of devices are comprised. There are two types of TCCSs (or TCCS circuits): those that couple the TC to a source supply, which may be called "charging TCCSs," and those that couple the TC to an output supply, which may be called "discharging TCCSs."

There is nothing ambiguous about the term "a TCCS circuit" as set forth in Claim 34. It is written to refer to one of the TCCS circuits previously introduced in Claim 28, or to another as-yet unidentified TCCS circuit. TCCS is simply shorthand for the phrase "transfer capacitor coupling switch."

A "switch circuit" need not be greatly different than a "switch." The terms may be redundant in some instances; but in other circumstances, a "switch circuit" may include a device that may be called a "switch," together with one or more additional devices, the combination constituting the "circuit." Thus, for example in FIG. 6, FET 602 together with resistor 626 might constitute a "switch circuit." As another example, it is known to "stack" a multiplicity of FETs together in series, each with its own bias resistor. The nodes of all bias resistors not connected to the gate of the corresponding FET are then tied together. Such a circuit can behave precisely as a single switch, and certainly constitutes a "switch circuit." However, a "switch" can also refer to such a switch circuit; it is merely a matter of connotation and convenience. Throughout a string of dependent claims, the language selected is used consistently, thus resulting in no "insoluble ambiguity," as required to reject claims for indefiniteness.

It is respectfully submitted that the foregoing remarks demonstrate that Claim 34 is clear as written. The language of Claim 34 is certainly sufficiently clear to allow those skilled in the charge

pump art to understand what is claimed when read in light of the specification. As such, the rejection of Claim 34 as undefined is improper. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 34.

VII.C.1.g Rejection of Claim 35 as Indefinite

The Examiner asks (Final Rejection, page 9 lines 7-9): "Similar to claim 34 above, how do the 'actively controlled TCCS circuits' of claim 35 relate to 'a TC-coupling switch ("TCCS") circuit' (lines 3-4), and 'a discharging TCCS circuit' (line 6), recited within claim 28?"

A TCCS circuit may be actively controlled (see FETs 602, 604, 608 and 610 of FIG. 6 and paragraph 54), or it may be passive (see diode-connected FETs 704 and 706 of FIG. 7 and paragraphs 60-61). Claim 35 recites in part (underlining added for emphasis): "wherein actively controlled TCCS circuits each have an associated control node, the method further comprising coupling the associated control node of each of the actively controlled TCCS circuits to the first charge pump clock output via a corresponding capacitive coupling circuit." The first underlined language defines actively controlled TCCS circuits as having a control node, and the second underlined language specifies (capacitive) coupling to such control nodes.

In view of the Examiner's evident discomfort with this concept, it is expressly observed that if the charge pump has no active TCCSs, (as is possible with "direct drive" charge pumps), then the limitation "each of the actively controlled TCCS circuits" would refer to a null set. Claim 35 is therefore irrelevant to charge pumps that have no actively-controlled TCCS circuits.

It is respectfully submitted that the language of Claim 35, as presently pending, is clear and unambiguous. Especially when read in light of Appellants' specification, Claim 35 is certainly sufficiently clear to allow those skilled in the charge pump art to understanding what is claimed. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 35.

VII.C.1.h Rejection of Claim 36 as Indefinite

The Examiner states (Final Rejection, page 9 lines 9-13, underlining added for emphasis): "It is not understood how "a particular first clock generator driver circuit" on line 4 of claim 36 relates

to "a first clock generator driver circuit is a driver circuit" recited on lines 1-2 of the same claim. For example, are both phrases referring to the exact same driver circuit, or does the first clock generator circuit comprise more than just "a first clock generator driver circuits?"

Claim 36 recites in part (underlining added for emphasis): "a first clock generator driver circuit is a driver circuit functionally incorporated in a first clock generator circuit configured to generate the first charge pump clock output, the method further comprising:" This is language definitional, preparatory to the body of Claim 36. As described in Appellant's specification, the preferred embodiment of a clock generator, for example, there are three driver circuits (see 502, 504 and 506 of FIG. 5). Because this is within "a first clock generator circuit," the drivers are each "first clock generator driver circuit[s]." This is admittedly not perfect prose, but it yields to careful parsing and is therefore not "insolubly ambiguous."

Claim 36 continues in further part: "c) limiting source currents from a particular first clock generator driver circuit by means of a first current limiting circuit; and d) limiting sink currents into the particular first clock generator driver circuit by means of a second current limiting circuit." Because there are typically a plurality of such "first clock generator driver circuits," clause (c) refers to "a particular" one of such drivers, thus enabling clause (d) to refer to the same driver circuit.

The language of Claim 36 is admittedly somewhat difficult, but it is not therefore ambiguous, and it is certainly not insolubly ambiguous, and thus is not indefinite. When read in light of Appellants' specification, Claim 36 certainly is sufficiently clear to allow those skilled in the charge pump art to understand what is claimed. Accordingly, the panel is respectfully requested to reverse the Examiner as to the rejection of Claim 36 as indefinite.

VII.C.1.i Rejection of Claim 39 as Indefinite

The Examiner states (Final Rejection, page 9 lines 14-17): "Related to claim 36's driver circuit problem above, it is not understood how claim 39's "all first clock generator driver circuits" relate to the singular "a first clock generator driver circuit", "a driver circuit", or "a particular first clock generator driver circuit" recited within claim 36."

As set forth above in regard to Claim 36, there are typically a plurality of "first clock generator" driver circuits (three, in a preferred embodiment). The term "All" refers to all of them. Claim 39 is easily understood once Claim 36 is parsed correctly. Claim 39 is thus unambiguous, wherefore the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 39.

VII.C.1.j Rejection of Claim 41 as Indefinite

The Examiner states (Final Rejection, page 9 lines 17-21): "It is not clear how "a passive TCCS circuit" in claim 41 relates to "a TC-coupling switch ("TCCS") circuit" (lines 3-4), or to "a discharging TCCS circuit" (line 6), recited within claim 28. Also, if a TCCS circuit is a switching circuit controlled by a charge pump clock, as identified within claim 28, how can it be considered "passive" as claim 41 recites with the "passive TCCS circuit" phrase."

The remarks set forth above (in this subsection) with regard to Claims 34 and 35 are believed to resolve all of the issues raised in the first of the Examiner's two sentences quoted immediately above. The remarks in respect of Claim 35 should also resolve the issues raised in the second sentence (see diode-connected FETs 704 and 706 of FIG. 7 and paragraphs 60-61). Diodes are switching devices that turn off and on according to the voltage impressed across them. The voltage impressed upon the diode-connected FETs 704 and 706 is provided by CLK 524 via the coupling capacitor 702, which is also the transfer capacitor. A thorough description of the characterization of diodes as "passive switches" is set forth in paragraphs 60-62 of Appellant's specification. Therefore, especially when read in light of Appellants' specification, the language of Claim 41 is sufficiently clear to allow those skilled in the charge pump art to understand what is claimed.

The remarks above confirm that Claim 41, as presently pending, is unambiguous in view of the specification, and is therefore not indefinite. Accordingly, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 41.

VII.C.1.k Rejection of Claim 42 as Indefinite

The Examiner states (Final Rejection, beginning page 9 last partial sentence): "Clarification is requested with respect to how the 'a discharging TCCS circuit' (line 6), 'a discharge common

TCCS' (on lines 10-11), and 'a discharge output TCCS' (line 13) within claim 42 relate to one another. For example, was 'TCCS' on each of lines 11, 13, 14, and 15 of claim 42 meant to be --TCCS circuit--, or is a 'TCCS' intended to be different from a 'TCCS circuit'?"

As described above in the remarks in respect of Claims 34 and 35, TCCSs (or TCCS circuits) may be divided into two categories: "charging" TCCSs that couple the TC to the source, and "discharging" TCCSs that couple the TC to the output. In a typical example, such as illustrated in FIG. 6, there are two of each of these types of TCCS.

Claim 42 further distinguishes between two different discharging TCCSs. Claim 42 clause (a) defines "a discharging TCCS circuit." Clause (c) further defines a "discharge common TCCS" as one that couples a terminal of the TC to an output common. Clause (d) further defines a "discharge output TCCS" as one that couples the opposite terminal of the TC to the output during discharging. Names are given to these circuits so that they can then be referenced and defined with respect to each other in clause (e). The language of Claim 42 is easily parsed when reviewed carefully.

While this may not be the very easiest way to describe complicated subject matter, there is no requirement in the law that claim language be perfect. Rather, as noted above, the claim must be sufficiently clear so as to allow those skilled in the art to understand what is claimed when the claim is read in light of the specification. It is therefore respectfully submitted that the language of Claim 42 is clear and unambiguous when read in light of Appellants' specification, and that it is therefore not "insolubly ambiguous." Consequently, Claim 42 is not indefinite, and the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 42.

VII.C.1.l Rejection of Claim 45 as Indefinite

The Examiner states (Final Rejection, page 10 lines 3-8): "It is not understood how claim 45's 'the driver output node' relates to 'each inverting driver output node' and 'each of the inverting driver output nodes' that are recited within claim 43 (e.g. see lines 5 and 8, respectively). For example, is one capacitor coupled to each output node; is each output node coupled to a corresponding capacitor; or is the capacitor coupled only to one particular output node that probably provides the clock output?"

Only one "driver output node of the first charge pump clock circuit" is referenced in Claims 43 and 45. Claim 45 requires coupling a capacitor to such output node (typically but not necessarily to ground) in order to limit voltage transition rates (*i.e.*, slow down the output).

Claim 43 recites in part (underlining added for emphasis):

> a) coupling the TC to the output supply during discharge periods via a discharging switch circuit under control of a first charge pump clock output;
> b) limiting source current provided to each inverting driver output node of a current-starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator circuit by means of a corresponding source current-limiting circuit; and
> c) limiting sink current drawn from each of the inverting driver output nodes by the driver circuit by means of a corresponding sink current-limiting circuit;
> d) wherein the inverting driver output node of one of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output.

Claim 45 recites in part (underlining added for emphasis): "... coupling a capacitor to the driver output node of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node."

Clause (d) of Claim 43 references "one of the ... inverting driver stages of the first charge pump clock generator circuit." Each such inverting driver stage has an inverting driver output node, as defined in clauses (b) and (c). Clauses (b) and (c) therefore specify an inverting driver node associated with each of the inverting stages in the ring oscillator. Accordingly, a definite article is warranted for (the) "inverting driver output node of" "one of the ... [stages]," as recited in Claim 45.

Though rather convoluted to achieve a specific concept, the language of Claim 45, taken together with Claim 43, is clearly unambiguous when reviewed by one skilled in the charge pump art. When Claim 43 is read in light of Appellants' specification, those skilled in the charge pump art will certainly understand what is defined. As such, Claim 45 is not indefinite, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 43 as indefinite.

VII.C.1.m Rejection of Claims 50-53 as Indefinite

The Examiner states that Claims 51-53 have the same problem as Claim 50. In regard to Claim 50, the Examiner states (Final Rejection, page 10 lines 8-13, underlining added):

> The coupling of the TC to the output supply "via a plurality of TC discharging switches" in claim 50 is confusing and/or misleading. This implies that more than one TC discharging switch couples the TC to the output supply. However, using the applicants' own figures as a reference, none of the figures show such a configuration. For example, even if switches 608 and 610 are considered as the discharging switches, only switch 610 actually connects TC 606 to output supply Vo-.

Every voltage supply has two terminals, even if one is common to another supply. In FIG. 6 of Appellants' specification, the output supply Vo- has a node that is tied to a node of the input supply. Both input and output are thus referenced to the same "common" voltage. This need not be the case, as may be seen in FIG. 9 and the associated text. In FIG. 6, the discharging TCCSs are 608 (which couples a first node of TC 606 to a first terminal of the output supply Vo-, namely common reference 404) and 610 (which couples the second node of TC 606 to the second node of the output supply Vo-).

Please refer to the remarks set forth above with respect to Claim 42 for further description. As described thereat, TCCS 608 is designated as the "discharge common" TCCS, while TCCS 610 is designated as the "discharge output" TCCS. Both are "discharge TCCSs." It is respectfully submitted that when Claims 50-53 are read in light of Appellants' specification, those skilled in the charge pump art will understand what is defined thereby. The skilled person will readily understand the foregoing, and the scope of Claims 51-53. As such, the rejections of Claims 50-53 as indefinite are unwarranted, and the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 50-53.

VII.C.1.n Rejection of Claim 56 as Indefinite

The Examiner's statement supporting the rejection of Claim 56 as indefinite indicates the same misunderstanding made with respect to Claim 35. As such, the remarks regarding Claim 35 (set forth above in this subsection) are also applicable here, and such remarks are incorporated herein. As noted there, TCCSs can be active or passive, as described and defined in paragraph 54 (actively controllable) and paragraphs 60-62 (passively controllable).

"Actively controllable" and "passive" switches will typically be understood by those of skill in the charge pump art, but the specification eliminates any possible ambiguity. The use of these well-defined terms permits the claims to be much more concise and comprehensible than would otherwise be the case.

The test for definiteness has long been whether one of skill in the art would understand the language when viewed in light of the specification. It is respectfully submitted that Claim 56 would thus be readily understood. Claim 56 is accordingly not indefinite. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 56.

VII.C.1.o Rejection of Claims 63 and 65 as Indefinite

The Examiner states (Final Rejection, page 11 lines 6-10): "The "additional second TC charging switch" of claim 63 is misleading and/or confusing. For example, where in the applicants' own figures is it shown, or where is it clearly disclosed, that there can be more than one switch coupled between the TC and the source voltage? For similar reasons, the "additional second TC discharging switch" of claim 65 is misleading and/or confusing."

These reasons for rejecting Claims 63 and 65 are substantially identical to the reasons provided by the Examiner for rejecting Claims 50-53. The remarks set forth above (in this subsection) in regard to Claims 50-53 address these reasons, and are incorporated here by reference.

It should be clear that each supply (input and output) has two terminals. In some instances, a TC might be coupled to an input or output supply by only one TCCS, but in a situation such as illustrated in the Appellants' FIG. 6, there are two TCCSs for each supply: two charging TCCSs

coupling the TC to the source supply, and two discharging TCCSs coupling the TC to the output supply.

The foregoing remarks, in conjunction with those set forth above with respect to Claims 50-53 above, support a conclusion that Claims 63 and 65 are clear and unambiguous. When Claim 63 and 65 are read in light of Appellants' specification, those skilled in the charge pump art will readily understand what is defined thereby. Because they are not indefinite, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 63 and 65.

VII.C.1.p Rejection of Claim 66 as Indefinite

The Examiner states (Final Rejection, page 11 lines 12-16, emphasis in original): "It is not clear how 'each actively controllable TC coupling switch' of claim 66 relates to the charging and discharging switches of claim 60. For example, is each switch within claim 60 inherently an 'actively controllable TC coupling switch', or can claim 66's 'each actively controllable TC coupling switch' be referring to switches other than the single 'TC charging switch' and 'TC discharging switch' of claim 60?"

Claim 60 can have a multiplicity of TC charging switches and a multiplicity of TC discharging switches. For example, consider the "stacked" embodiment shown in FIG. 9 of Appellants' specification. In accordance with that embodiment, either additional output voltages, or a single larger-magnitude output voltage, can be produced.

Claim 66 recites in part (underlining added for emphasis): "capacitively coupling a control node of each actively controllable TC coupling switch that is incorporated within a charge pump to a corresponding charge pump clock output."

As remarked above with respect to the indefiniteness rejections of Claims 35 and 56, TCCSs may be either actively controllable, or passive (see paragraphs 54 and 60-62 of Appellants' specification). If all switches of an embodiment are passive, such as is the case with diodes, then Claim 66 is not relevant. However, if an embodiment includes actively controllable TCCSs, Claim

66 requires them to be capacitively coupled to the charge pump clock. Claim 66 permits the use of multiple different clocks.

It is respectfully submitted that Claim 66, as presently pending, is unambiguous. Those skilled in the charge pump art will readily understand what is defined by Claim 66, especially when this claim is read in light of Appellants' specification. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 66.

VII.C.1.g Rejection of Claims 13, 43, 46-48, 60 and 62 as Indefinite

These claims can admittedly benefit from enhancements in clarity. However, that does not mean that they are "insolubly ambiguous" and therefore indefinite. Each claim is addressed in turn below:

Claim 13: It is agreed that that the term --charge pump clock output-- is clearer than the present recital of "driver output node" in Claim 13, but respectfully submitted that the present language is not "insolubly ambiguous" to one of skill in the art. Granting that clarity could be enhanced, it is respectfully proposed that the panel deem Claim 13 allowable contingent upon amending the claim to replace each instance of the phrase "driver output node" with the phrase --charge pump clock output --.

Claim 43: In clause (c) of Claim 43, the phrase "by the driver circuit" does not belong, and should be deleted, though its presence does not necessarily render the claim insolubly ambiguous to one of skill in the charge pump art, who would recognize it as a typographical error. Clause (d) should not be labeled with a letter at all, which would obviate the conflict of Claim 43 with Claim 42 due to a different clause that is also labeled "(d)". It is respectfully submitted that, though the label error might cause a reader to pause, it would not necessarily render the claim insolubly ambiguous. To improve the clarity, however, it is respectfully proposed that the panel deem Claim 43 allowable, contingent upon deleting the label "d)" from the last clause, and also deleting the phrase "by the circuit driver" from clause (c).

Claims 46 and 47: Both of these claims include a very slight antecedent basis error: the phrase "the discharging switch" should be replaced by the phrase --the discharging switch circuit--, in order to be completely consistent with Claim 43 from which these claims depend. However, such error does not render the claims indefinite. "When the meaning of the claim would reasonably be understood by persons of ordinary skill when read in light of the specification, the claim is not subject to invalidity upon departure from the protocol of "antecedent basis." *Energizer Holdings, Inc. V. International Trade Commission*, 435 F.3d 1366[21]. Because the meaning of Claims 46 and 47 would be readily understood by persons of ordinary skill in the charge pump art, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 46 and 47. However, admittedly, Claims 46 and 47 could easily be improved. Accordingly, it is respectfully proposed that the panel deem Claims 46 and 47 allowable contingent upon replacing each instance of "switch" with the term --switch circuit-- in both claims, thereby achieving consistency with both Claim 43, from which they depend, and with the terminology of related Claim 44 (which recites "charging switch circuit"). Such amendments would overcome the Examiner's legitimate concerns.

Claim 48: Claim 48 recites in part: " ... coupling the first charge pump output as a signal to a control node of the discharging switch circuit ... ." Because Appellants' specification frequently addresses coupling charge pump clock outputs to control nodes of switch circuits (TCCSs), and because a person of ordinary skill in the charge pump art would understand that coupling a "charge pump output" to a control node of such a switch is not shown anywhere in the specification, such a skilled person would deduce (admittedly, with some effort) that the phrase "charge pump output" should be interpreted as --charge pump clock output--. "[I]f the meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons will disagree, we have held the claim sufficiently clear to avoid invalidity on indefiniteness grounds." *Energizer v. ITC, id.*, endnote 21. Under this standard, Claim 48 is not indefinite when read in light of Appellants' specification. However, acknowledging that the claim as written is far less clear than is desirable, it is respectfully proposed that the panel deem Claim 48 allowable

contingent upon replacing the phrase "charge pump output" with the phrase --charge pump clock output--.

Claim 60: The preamble of Claim 60 recites in part: "A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge for the output from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply ..." It is acknowledged that the first instance of "the output" lacks antecedent basis because the term "output" is not followed by the term --supply--. While the error does not render Claim 60 indefinite (*see, e.g., Energizer v. ITC, id.*, endnote 21.), correction is preferred. Accordingly, it is respectfully proposed that the panel deem Claim 60 allowable contingent upon inserting the term "supply" after the second instance of the term "output."

Claim 62: Claim 62 recites: "The method of Claim 61, further comprising biasing each of the capacitive coupling networks such that the switch device to which it is coupled is nonconductive when the charge pump clock output is at an average voltage." It is respectfully submitted that this language is unambiguous in view of Claim 60, from which it depends. Claim 60 specifies coupling "to a control node of a TC charging switch via a first capacitive coupling network," and coupling "to a control node of a TC discharging switch via a second capacitive coupling network." Thus, because signals are coupled thereby, each capacitive coupling network is necessarily coupled to either a charging switch (control node), or to a discharging switch (control node). As such, "the switch device" to which each capacitive coupling network is coupled is readily understood, and the claim is not "insolubly ambiguous" merely because the switch was subsequently designated as a "switch device." Nonetheless, improvement is desirable and amendment of the claim would overcome the Examiner's legitimate concerns. Accordingly, it is respectfully proposed that Claim 62 be held allowable contingent upon replacing the phrase "coupling networks such that the switch device to which it is coupled" with the phrase --coupling networks such that the TC charging or discharging switch to which it is coupled--. The proposed changes are as follows: "coupling networks such that the TC charging or discharging switch ~~device~~ to which it is coupled."

Conclusion

The evidence, law and arguments set forth above address every ground of rejection under 35 USC 102 or 103. Law and arguments are also set forth above that support a conclusion that the Examiner should be reversed as to most of the rejections under 35 USC 112, second paragraph, and such reversal as to each ground of objection thus addressed is respectfully requested.

It is again respectfully submitted that the proffered Amendment After Final Rejection should be entered as placing all claims of the application into condition for allowance.

The Commissioner is requested to construe this Appeal Brief as including a petition to extend the period for submission under 37 CFR 1.136(a) by the number of months necessary to make this submission timely filed. Fees or deficiencies required to cause this Appeal Brief to be complete and timely filed may be charged, and any overpayments should be credited, to our Deposit Account No. **50-0490**.

Respectfully submitted,

1/5/2007
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VIII. CLAIMS APPENDIX

1. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output; and

c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes

i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and

ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output;

d) wherein the plurality of transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times.

2. The apparatus of Claim 1, wherein the plurality of transfer capacitor coupling switches are under control of the particular charge pump clock output.

3. The apparatus of Claim 2, further comprising coupling circuitry configured to couple the particular charge pump clock output as a signal to each of the transfer capacitor coupling switches without increasing a rate of voltage rise or fall of the signal.

4. The apparatus of Claim 1, further comprising a coupling circuit configured to couple the particular charge pump clock output as a signal to the at least one transfer capacitor coupling switch without increasing a rate of voltage rise or fall of the signal.

5. The apparatus of Claim 1, further comprising a capacitive coupling circuit configured to couple one of the at least one charge pump clock outputs to a control node of one of the plurality of transfer capacitor coupling switches.

6. The apparatus of Claim 2, further comprising corresponding capacitive coupling circuits to couple a control node of each of the plurality of transfer capacitor coupling switches to the particular charge pump clock output.

7. The apparatus of Claim 6, wherein none of corresponding capacitive coupling circuits is configured to conduct substantial charge to the transfer capacitor.

8. The apparatus of Claim 5, wherein the capacitive coupling circuit does not conduct substantial charge to the transfer capacitor.

9. The apparatus of Claim 1, wherein the active current limit circuitry of (c)(i) and (c)(ii) is further configured to limit source and sink currents, conducted by each driver section within the charge pump clock generating circuit, to substantially identical magnitudes.

10. The apparatus of Claim 1, further comprising coupling substantial charge into the transfer capacitor via the charge pump clock output.

11. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of a charge pump clock output and including

i) a common discharge switch disposed between a terminal of the transfer capacitor and a common reference connection of the output voltage supply, and having a first control node AC impedance, and

ii) an output supply discharge switch disposed between an opposite terminal of the transfer capacitor and a connection of the output voltage supply opposite the common reference connection, and having a second control node AC impedance at least twice the first control node AC impedance; and

c) a charge pump clock generating circuit including

i) circuitry configured to limit a rate of rise of the charge pump clock output, and

ii) circuitry configured to limit a rate of fall of the charge pump clock output;

d) wherein the transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times.

12. Charge pump apparatus within a monolithic integrated circuit for generating an output voltage supply, comprising:

a) a transfer capacitor coupled alternately between source connections and output connections;

b) a plurality of active switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output to couple charge, which is not substantially conducted by the charge pump clock output, from the source connections to the output connections;

c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to

i) circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and

ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

13. The apparatus of Claim 12, wherein the charge pump clock generating circuit c) further comprises a discrete capacitive element coupled to the driver output node and configured to reduce voltage rates of change at the driver output node.

14. The apparatus of Claim 12, wherein the charge pump clock generating circuit includes a plurality of active driver circuits configured to both source and sink current with respect to a corresponding driver output node, and wherein the charge pump clock generating circuit includes circuitry to limit the current source capacity of each of the active driver circuits and circuitry to limit the current sink capacity of each of the active driver circuits with respect to the corresponding driver output node.

15. The apparatus of Claim 12, further comprising one or more capacitive coupling networks configured to couple one of the at least one charge pump clock outputs to a control node of an active switch.

16. The apparatus of Claim 12, wherein the charge pump clock generating circuit is configured as a current-starved ring oscillator.

17. The apparatus of Claim 12, wherein the source current circuitry c) i) and the sink current circuitry c) ii) are configured to limit source and sink currents to a substantially identical magnitude.

18. Charge pump apparatus for generating an output voltage supply within a monolithic integrated circuit, comprising:

a) a transfer capacitor;

b) one or more source switching devices disposed in series between the transfer capacitor and a voltage source to convey transfer current to the transfer capacitor from the voltage source when conducting;

c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply to convey transfer current from the transfer capacitor to the output voltage supply when conducting; and

d) a charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.

19. The apparatus of Claim 18, further comprising a second charge pump stage including:

e) a second transfer capacitor;

f) one or more second-source switching devices disposed in series between the second transfer capacitor and a second voltage source; and

g) one or more second-output switching devices disposed in series between the second transfer capacitor and a second output voltage supply;

h) wherein the charge pump clock output is coupled to all of the second-source switching devices to cause conduction during the charge periods and nonconduction during the discharge periods, and is coupled to all of the second-output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods.

20. The apparatus of Claim 18, further comprising circuitry configured to reduce voltage change rates of the charge pump clock output during both positive and negative transitions compared to an absence of such circuitry such that the charge pump clock output voltage is substantially sine-like.

21. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) one or more source switching devices disposed in series between the transfer capacitor and a voltage source;

c) a first output switching device having a first device area disposed between a first terminal of the transfer capacitor and the output voltage supply, and a second output switching device disposed between a common reference connection of the output voltage supply and a second terminal of the transfer capacitor opposite the first terminal of the transfer capacitor, having a second device area that is greater than double the first device area; and

d) a charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled to all of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled to all of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices.

22. The apparatus of Claim 18, wherein the charge pump clock generating circuit (d) further comprises circuitry configured to limit currents conducted by each amplifying driver circuit in the charge pump clock generating circuit.

23. The apparatus of Claim 22, further comprising a discrete capacitive device coupled to an output of one of the amplifying driver circuits to limit a rate of voltage change of the driver circuit output.

24. Charge pump apparatus for generating an output voltage supply within a monolithic integrated circuit, comprising:

a) a transfer capacitor for conveying charge from a voltage source to the output voltage supply;

b) one or more source switching devices disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;

c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source; and

d) a capacitive coupling circuit coupling a charge pump clock output to one of the control nodes corresponding to a source switching device or to an output switching device.

25. The apparatus of Claim 24, wherein the capacitive coupling circuit is a first capacitive coupling circuit coupling the charge pump clock output to a source switching device control node, and further comprising a second capacitive coupling circuit coupling the charge pump clock output to an output switching device control node.

26. The apparatus of Claim 25, wherein each of the capacitive coupling circuits includes biasing circuitry configured such that an average control voltage causes a switching device to which it is coupled to be substantially nonconductive.

27. The apparatus of Claim 25, wherein all source switching devices disposed in series between the transfer capacitor and the voltage source, and all output switching devices disposed in series between the transfer capacitor and the output voltage, are capacitively coupled to the charge pump clock output.

28. A method of generating an output supply from a charge pump incorporated within a monolithic integrated circuit by transferring charge from a source voltage to a transfer capacitor ("TC") alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit is a switching circuit of the charge pump configured to couple the TC to a supply under control of a charge pump clock, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging TCCS circuit under control of a first charge pump clock output; and

b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions such that a voltage of the first charge pump clock output is substantially sine-like.

29. The method of Claim 28, further comprising

c) coupling the TC to the source voltage via a charging TCCS circuit, under control of a second charge pump clock output, during charge periods that nonoverlappingly alternate with the discharge periods; and

d) actively limiting a rate of voltage change of both positive and negative transitions of the second charge pump clock output.

30. The method of Claim 29, wherein the first charge pump clock output is the second charge pump clock output.

31. The method of Claim 30, further comprising controlling all TCCS circuits by means of the first charge pump clock output.

32. The method of Claim 31, further comprising coupling the TC to a connection of the source voltage during a charging period via the charge pump clock output.

33. The method of Claim 28, further comprising limiting a current drive capacity of the charge pump clock output by means of a current limiting circuit.

34. The method of Claim 28, further comprising coupling the first charge pump clock output to a control node of a TCCS circuit via a capacitive coupling circuit.

35. The method of Claim 28, wherein actively controlled TCCS circuits each have an associated control node, the method further comprising coupling the associated control node of each of the actively controlled TCCS circuits to the first charge pump clock output via a corresponding capacitive coupling circuit.

36. The method of Claim 28, wherein a first clock generator driver circuit is a driver circuit functionally incorporated in a first clock generator circuit configured to generate the first charge pump clock output, the method further comprising:

c) limiting source currents from a particular first clock generator driver circuit by means of a first current limiting circuit; and

d) limiting sink currents into the particular first clock generator driver circuit by means of a second current limiting circuit.

37. The method of Claim 36, further comprising limiting the source currents and the sink currents of the particular first clock generator driver circuit to substantially identical magnitudes.

38. The method of Claim 36, wherein the first current limiting circuit comprises a current mirror device, and the second current limiting circuit comprises a different current mirror device.

39. The method of Claim 37, further comprising limiting source currents and sink currents from all first clock generator driver circuits.

40. The method of Claim 28, further comprising generating the first charge pump clock output by means of a current-starved ring oscillator including not more than three inverting driver sections coupled in a ring.

41. The method of Claim 28, further comprising coupling the TC to the source voltage or to the output supply in part via a passive TCCS circuit.

42. A method of generating an output supply from a charge pump by transferring charge from a source voltage to a transfer capacitor ("TC") alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit is a switching circuit of the charge pump configured to couple the TC to a supply under control of a charge pump clock, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging TCCS circuit under control of a first charge pump clock output;

b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions;

c) coupling a first terminal of the TC to a common reference connection of the output supply via a discharge common TCCS;

d) coupling a second opposite terminal of the TC to an output supply connection opposite the common reference connection via a discharge output TCCS; and

e) fabricating the discharge output TCCS to have a control node AC impedance at least double a control node AC impedance of the discharge common TCCS.

43. A method of generating an output supply by alternately transferring charge from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging switch circuit under control of a first charge pump clock output;

b) limiting source current provided to each inverting driver output node of a current-starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator circuit by means of a corresponding source current-limiting circuit; and

c) limiting sink current drawn from each of the inverting driver output nodes by the driver circuit by means of a corresponding sink current-limiting circuit;

d) wherein the inverting driver output node of one of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output.

44. The method of Claim 43, further comprising

d) coupling the TC to the source voltage via a charging switch circuit, under control of a second charge pump clock output, during charge periods alternating nonconcurrently with the discharge periods.

45. The method of Claim 43, further comprising coupling a capacitor to the driver output node of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node.

46. The method of Claim 43, further comprising coupling the first charge pump clock output to a control node of the discharging switch and/or to a control node of a charging switch via a corresponding capacitive coupling circuit.

47. The method of Claim 45, further comprising coupling the first charge pump clock output to a control node of the discharging switch and/or to a control node of a charging switch via a corresponding capacitive coupling circuit.

48. The method of Claim 43, further comprising coupling the first charge pump output as a signal to a control node of the discharging switch circuit via a network that is not configured to increase rates of voltage change of the signal.

49. A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

50. The method of Claim 49, wherein step a) further comprises coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output.

51. The method of Claim 50, wherein step b) further comprises coupling the TC to a voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output.

52. A method of generating an output supply by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output;

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output;

c) coupling a first TC discharging switch device in series between a first node of the TC and a common reference connection of the output supply;

d) coupling a second TC discharging switch in series between a second node of the TC opposite the first node and a connection of the output supply opposite the common reference connection; and

e) fabricating the second TC discharging switch to have a control node AC impedance at least twice as large as a control node AC impedance of the first discharging switch.

53. The method of Claim 49, wherein step b) further comprises coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output.

54. The method of Claim 49, further comprising:

c) coupling a second TC to a second voltage source via a second TC charging switch under control of the charge pump clock output; and

d) coupling the second TC to a second output supply via a second TC discharging switch under control of the charge pump clock output.

55. The method of Claim 54, further comprising coupling the charge pump clock output to a control node of each TC charging switch, and to a control node of each TC discharging switch, via corresponding capacitive coupling circuits.

56. The method of Claim 49, further comprising coupling the charge pump clock output to a control node of each actively controllable TC charging switch, and to each actively controllable TC discharging switch, via corresponding capacitive coupling circuits.

57. The method of Claim 49, further comprising incorporating circuitry to reduce voltage change rates during both positive and negative transitions of the charge pump clock output.

58. The method of Claim 49, further comprising:

c) generating the charge pump clock output in a charge pump clock generator circuit having one or more driver circuits, and

d) limiting currents output from each driver circuit of the charge pump clock generator circuit.

59. The method of Claim 58, further comprising:

e) limiting rates of both positive and negative voltage transitions at an output node of one of the driver circuits of the charge pump clock generator circuit by coupling a capacitor to the output node of the driver circuit.

60. A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge for the output from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling a first charge pump clock output to a control node of a TC charging switch via a first capacitive coupling network that does not conduct a significant portion of the charge for the output;

b) coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output;

c) coupling a second charge pump clock output to a control node of a TC discharging switch via a second capacitive coupling network that does not conduct a significant portion of the charge for the output; and

d) coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output.

61. The method of Claim 60, wherein the second charge pump clock output is the first charge pump clock output.

62. The method of Claim 61, further comprising biasing each of the capacitive coupling networks such that the switch device to which it is coupled is nonconductive when the charge pump clock output is at an average voltage.

63. The method of Claim 62, further comprising coupling the TC to the source voltage during the charge periods via an additional second TC charging switch having a control node capacitively coupled to a corresponding second charge pump output.

64. The method of Claim 63, wherein the TC discharging switch is a first TC discharging switch and is coupled between a first node of the TC and a connection of the output supply opposite a common reference, the method further comprising coupling an opposite second node of the TC to a common reference of the output supply during the discharge periods via a second TC discharging switch having a control node AC impedance no more than half as large as a control node AC impedance of the first TC discharging switch.

65. The method of Claim 62, further comprising coupling the TC to the output supply during the discharge periods via an additional second TC discharging switch having a control node capacitively coupled to a corresponding second charge pump output.

66. The method of Claim 60, further comprising capacitively coupling a control node of each actively controllable TC coupling switch that is incorporated within a charge pump to a corresponding charge pump clock output.

67. The method of Claim 66, wherein all of the corresponding charge pump clock outputs are a common single-phase output.

IX. EVIDENCE APPENDIX

The following references relied upon by the Appellants were entered into the record at least when considered by the Examiner on the dates indicated. A copy of each reference is attached.

Each of the following references was cited in an Information Disclosure Statement filed in the U.S. Patent Office on February 10, 2004 and considered by the Examiner on November 17, 2004:

1. U.S. Patent No. 5,465,061, issued 11/7/95 to Dufour.
2. U.S. Patent No. 6,411,531, issued 6/25/02 to Nork, et al.
3. U.S. Patent No. 6,518,829, issued 2/11/03 to Butler.
4. Maxim Integrated Products, "Charge Pumps Shine in Portable Designs", published March 15, 2001, pages 1-13.
5. Texas Instruments, "TPS60204, TPS60205, Regulated 3.3-V, 100-mA Low-Ripple Charge Pump, Low Power DC/DC Converters", published February, 2001, Revised September 2001, pages 1 -18.
6. Sam Nork, "New Charge Pumps Offer Low Input and Output Noise" Linear Technology Corporation, Design Notes, Design Note 243, published November 2000, pages 1-2
7. Linear Technology, "LTC1550l/LTC1551L: Low Noise Charge Pump Inverters in MS8 Shrink Cell Phone Designs", published December 1998, pages 1-2
8. Lance Lascari, "Accurate Phase Noise Prediction in PLL Synthesizers", Applied Microwave & Wireless, pages 90-96, published May 2000.

Each of the following references were cited in an Office Action by Examiner Terry Englund from the U.S. Patent Office on December 1, 2004:

9. U.S. Patent No. 5,446,418, issued 8/29/95 to Hara, et al.
10. U.S. Patent No. 5,734,291, issued 3/31/98 to Tasdighi, et al.
11. U.S. Patent No. 6,400,211, issued 6/4/02 to Yokomizo, et al.
12. U.S. Patent No. 6,617,933, issued 9/9/03 to Ito, et al.

Each of the following references were cited in a Supplemental Information Disclosure Statement filed in the U.S. Patent Office on April 1, 2005, and were considered by the Examiner on June 26, 2005:

13. U.S. Patent No. 4,621,315, issued 11/4/86 to Vaughn, et al.
14. U.S. Patent No. 4,633,106, issued 12/30/86 to Backes, et al.
15. U.S. Patent No. 4,703,196, issued 10/27/87 to Arakawa.
16. U.S. Patent No. 4,752,699, issued 6/21/88 to Cranford Jr., et al.
17. U.S. Patent No. 4,769,784, issued 9/6/88 to Doluca, et al.
18. U.S. Patent No.4,777,577, issued 10/11/88 to Bingham, et al.
19. U.S. Patent No.4,897,774, issued 1/30/90 to Bingham, et al.
20. U.S. Patent No. 5,038,325, issued 8/6/91 to Douglas, et al.
21. U.S. Patent No. 5,068,626, issued 11/26/91 to Takagi, et al.
22. U.S. Patent No. 5,081,371, issued 1/14/92 to Wong.
23. U.S. Patent No. 5,111,375, issued 3/5/92 to Marshall.
24. U.S. Patent No. 5,126,590, issued 6/30/02 to Chern.
25. U.S. Patent No. 5,138,190, issued 8/11/92 to Yamazaki, et al.
26. U.S. Patent No. 6,130,572, issued 10/10/00 to Ghilardelli, et al.
27. U.S. Patent No.6,816,000, issued 11/9/04 to Miyamitsu.
28. U.S. Patent No. 6,816,001, issued 11/9/04 to Khouri, et al.
29. U.S. Patent No. 6,825,730, issued 11/30/04 to Sun.
30. U.S. Patent No.6,831,847, issued 12/14/04 to Perry.

Each of the following references were cited in an Office Action by Examiner Terry Englund from the U.S. Patent Office on August 10, 2005:

31. U.S. Patent No. 6,064,275, issued 5/16/00 to Yamauchi.
32. U.S. Patent No. 6,081,165, issued 6/2700 to Goldman.

X. RELATED PROCEEDINGS APPENDIX

None.

Charge Pumps Shine in Portable Designs

New-generation ICs have combined with passive-component improvements to make charge-pump voltage conversion a favored approach in many applications. In many cases, the earlier charge pumps were considered either unsuitable or acceptable only with compromise. For example, an application that had relaxed accuracy, low load current, high noise tolerance, and minimal need for efficiency could benefit from a charge pump's lower cost, smaller size, simpler circuitry, and-of course-inductor-free operation.

Today's charge-pump ICs meet the demanding requirements of portable systems with improved precision, higher output current, output noise levels acceptable to sensitive RF applications, and battery life comparable to that of some inductor-based designs. The following discussion compares several IC charge-pump designs, presents "inductorless" power-supply applications, and offers guidelines for component selection.

A short primer

The term "charge pump " refers to a type of dc-dc voltage converter that uses capacitors rather than inductors or transformers to store and transfer energy. Charge pumps (often called switched-capacitor converters) include a switch or diode network that charges and discharges one or more capacitors. The most compelling advantage of a charge-pump circuit is the absence of inductors.

Why avoid inductors? Compared with capacitors, they have fewer purchasing sources, fewer standard specifications and dimensions, greater component height, more EMI, greater layout sensitivity, and higher cost. (Otherwise, they're great.) The newer generation of charge-pump ICs offers satisfactory operation even with the low-cost ceramic capacitors commonly used to bypass power supplies.

The basic charge pump can be implemented in an IC with analog switches, or in a discrete-component circuit with diodes (**Figure 1**). In the IC version, the switch network toggles between charge and discharge states, and in the discrete version, the clock waveform drives the charge and discharge states via diodes. In both cases the "flying capacitor " (C1) shuttles charge, and the "reservoir capacitor " (C2) holds charge and filters the output voltage. You can expand and modify this scheme as required to add regulation, reduce noise, obtain higher output voltage, etc.

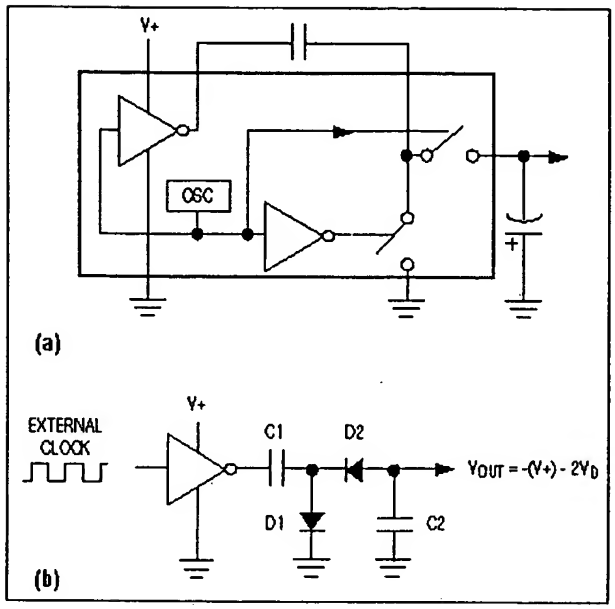


*Figure 1. A basic charge pump provides voltage doubling or inversion. It can be implemented with on-chip switches (**a**) or discrete diodes (**b**).*

Though charge pumps often serve as power sources for small circuit blocks or individual components such as interface ICs, they have not been widely used as system power supplies. This usage is changing, however: the output-current capability of charge pumps is increasing while the supply current required in portable designs is decreasing. In **Figure 2**, for example, the IC1 charge pump can generate 100mA at 3.3V when powered from a 2-cell battery of AA or AAA alkaline, NiCd, or NiMH cells, or a single primary lithium cell.

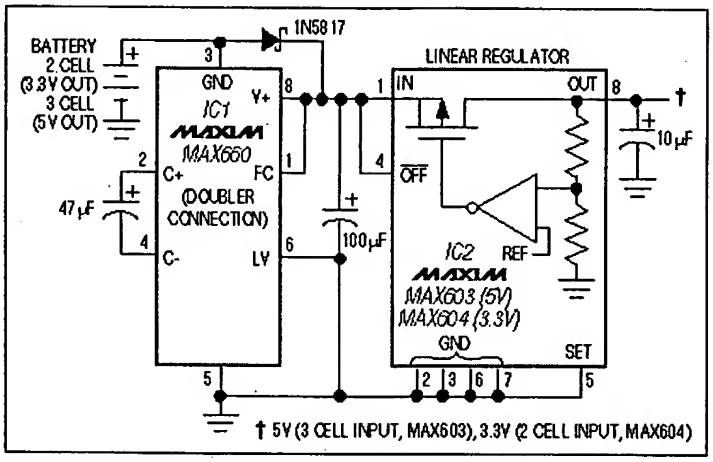


Figure 2. This charge-pump boost converter with linear regulator supplies 200mA at 3.3V with a 2-cell input, and 150mA at 5V with a 3-cell input.

The Figure 2 circuit can maintain its 3.3V output for inputs as low as 2.2V. For inputs ≥2.4V, it can supply short-term loads exceeding 200mA. For 5V systems with inputs as low as 3V, a similar design plus a 5V linear regulator supplies 150mA when powered from a 3-cell alkaline, NiCd, or NiMH battery, or one rechargeable lithium cell. The efficiency in both circuits varies from almost

80% (with low VIN) to slightly more than 50% when the battery voltage is high (3.2V for two cells, or 4.8V for three cells).

Internally regulated charge pumps

The Figure 2 circuit overcomes the charge pump's lack of regulation by adding a regulator externally. Another option-if load currents are modest-is to add regulation on the chip. Regulation in a monolithic chip is generally accomplished either as linear regulation or as charge-pump modulation. Linear regulation offers the lowest output noise, and therefore provides better performance in (for example) a GaAsFET-bias circuit for RF amplifiers. Charge-pump modulation (which controls the switch resistance) offers more output current for a given die size (or cost), because the IC need not include a series pass transistor.

The circuit of **Figure 3** is useful both in main supplies and in backup supplies. It generates a regulated 5V output for load currents to 20mA and inputs ranging from 1.8V to 3.6V. For input voltages no lower than 3V, the output current can reach 50mA. The conversion efficiency (**Figure 4**) approaches that of an equivalent low-cost, inductor-based circuit. Note the variation with input voltage: efficiency exhibits a step change near VIN = 3V, where the charge pump shifts automatically between its voltage-tripler and voltage-doubler modes of operation. For each "zone" of doubler or tripler operation, the highest efficiency occurs at the lowest VIN. Within each zone, the efficiency declines as the losses increase with VIN:

Power lost = I_{OUT} x [(2 or 3)V_{IN} - V_{OUT}].

The Figure 3 circuit accomplishes regulation without a linear pass element, but its losses are the same as those of an unregulated doubler or tripler feeding into a linear regulator! This surprising result is a consequence of the unavoidable loss that occurs whenever the pump capacitors change voltage within a switching cycle. Consider two 1μF capacitors, one charged to 1V and one to 0V. Their total stored energy is:

$1/2CV^2 = 1/2(1\mu F)(1V^2) + 1/2(1\mu F)(0V^2) = 0.5\mu$Coulombs.

Connecting them in parallel recharges each to 0.5V, so the new total is:

$1/2(1\mu F)(0.5V^2) + 1/2(1\mu F)(0.5V^2) = 0.25\mu$Coulombs.

Thus, the energy lost in going from 1V to 0.5V (50%) is the same as that expected from a fixed-VOUT doubler or tripler followed by a linear regulator. In Figure 3, efficiency is optimized by automatic shifts between doubler and tripler operation, which minimize the ΔV changes.

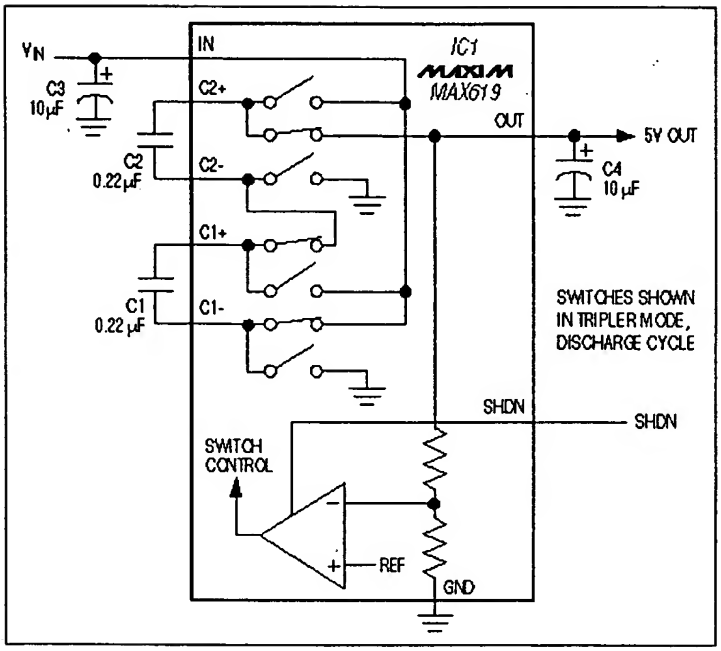


Figure 3. This IC contains a multi-switch boost converter with output regulation. The circuit either doubles or triples VIN to maximize efficiency. Switch-control information is fed back to maintain the output regulation.

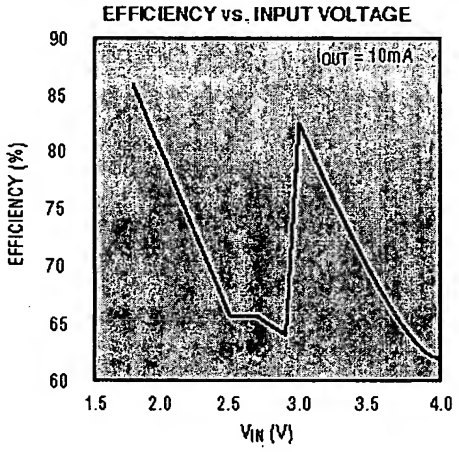


Figure 4. Discontinuities in the efficiency/VOUT profile for Figure 3 occur when the internal charge pump shifts between voltage doubling and tripling.

Operating current

Many capacitor-based voltage converters offer extremely low operating current-a useful feature in systems for which the load current is either uniformly low, or low most of the time. Thus, for smaller hand-held products the light-load operating currents can be much more important than full-load efficiency in determining battery life. In such products, the "off" state is not completely off, but rather a suspend or sleep state in which the supply current required (for µP and memory, for instance) may be 100µA or less. Battery life is affected directly if a comparable current is drawn by the power supply itself.

The supply current for a charge-pump IC is generally proportional to its operating frequency. You can minimize the current draw by running at the lowest possible frequency, but the penalty (for older charge-pump ICs) is higher ripple voltage, less IOUT capability, and the need for larger valued pump capacitors. Some ICs provide a pin-settable operating frequency to assist in making this tradeoff.

Newer charge-pump ICs employ another technique (on-demand switching), which enables low quiescent current and high-IOUT capability at the same time. Thus, the Figure 3 system incorporates on-demand circuitry that lowers the no-load supply current to 75μA (typical).

Although Figure 3's full-load efficiency (shown in Figure 4) is less than that found in most inductor-based designs, its very low operating current may allow a longer battery life. The effect of operating current on battery life depends on the fraction of operating time spent in the suspend or sleep state. The MAX619 in Figure 3, for instance, includes an on-demand oscillator that runs only when the output voltage falls below 5V. The resulting no-load quiescent current is only 75μA, and the device delivers output currents to 50mA using 0.22μA pump capacitors. Low operating current is also of interest when generating a backup voltage for lithium coin cells.

Flash memory

An application well suited for charge-pump conversion is the generation of a programming voltage for flash memory chips. The charge-pump approach provides a nearly ideal solution for credit-card-sized products in which the component height is severely restricted-particularly if it lowers the number of electrolytic capacitors or eliminates them altogether. An IC designed for this purpose (**Figure 5**) supplies a 12V "VPP" voltage suitable for programming 2-byte words of flash memory. Another IC (the MAX619, mentioned earlier) supplies a 5V VPP for 5V flash devices.

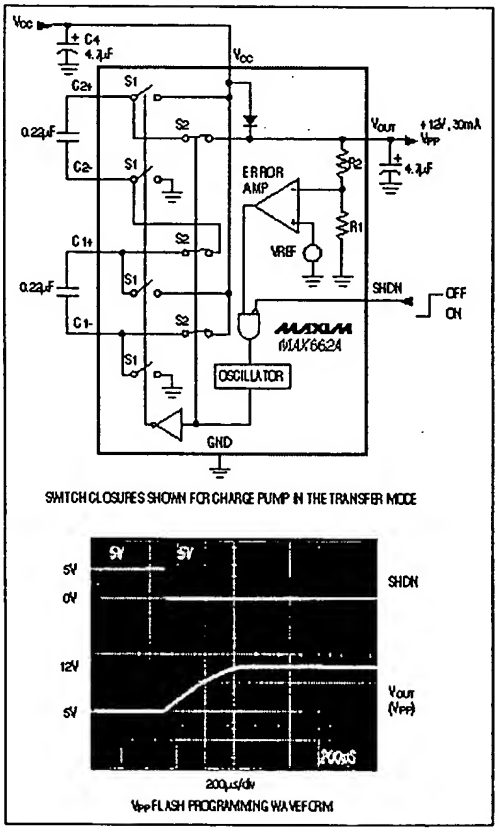


Figure 5. This IC generates the VPP programming voltage required for a 12V flash memory (12V). VOUT is fully regulated for loads of 30mA.

Compared with other types of voltage converters, the charge pump can provide superior performance in applications that process low-level signals or require low-noise operation. In some cases, the charge pump now allows voltage conversion in applications for which the only feasible solution had been a linear regulator. Note that these advantages don't apply to all charge pumps. When compared with inductor-based circuits, some disadvantages become apparent as well.

The most direct advantage is elimination of the magnetic fields and EMI that come with an inductor or transformer. One EMI source remains in a charge-pump circuit-the high charging current that flows to a "flying capacitor" when it connects to an input source or another capacitor with a different voltage. The instantaneous current flow is limited only by the associated capacitor ESR and switch resistance, which can be as low as 5Ω. Unless the charge pump is tailored for low-noise operation, the noise produced by these high-$\Delta I/\Delta t$ events can be eliminated only by post filtering or a large capacitance.

One example of a low-noise charge-pump converter is the MAX850 (**Figure 6**). Designed to generate very quiet negative bias voltages for GaAsFET RF power amplifiers, it combines an inverting charge pump with a low-noise, negative-output linear regulator. The MAX850 operates from 5VDC and has a high switching frequency (100kHz) that enables the use of small-valued external capacitors. An on-chip regulator lowers the output ripple and noise to only 2mVp-p. This noise (**Figure 7**) is remarkably low for a switching power supply.

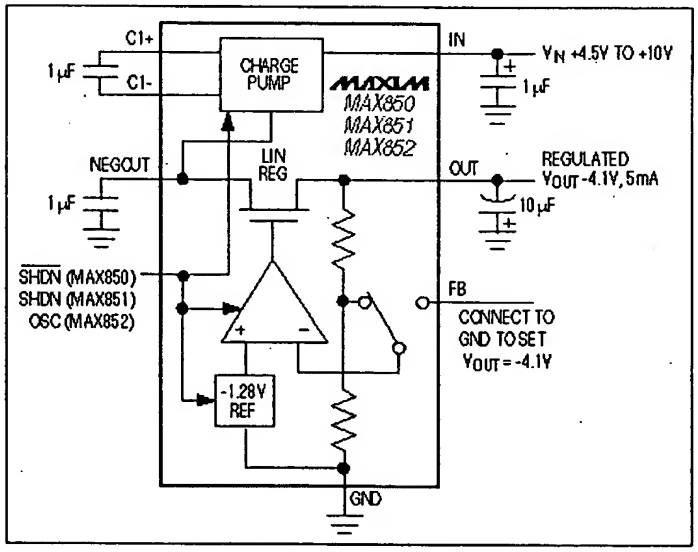


Figure 6. This GaAsFET-bias power supply contains a linear regulator that limits the output noise to 2mVp-p.

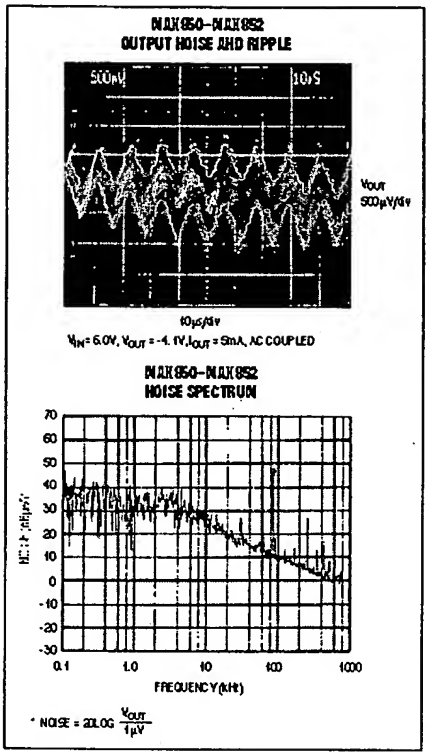


Figure 7. This noise plot for the Figure 6 circuit shows noise below 2mVp-p.

A similar approach taken in higher-current applications supplies a low-noise bias for the magneto-resistive read-write head in a high-capacity (2Gbytes and up) hard-disk drive. Such drives typically require -3V at 100mA, with no more than 10mVp-p of output noise and ripple. The pump output's switching transients again preclude a direct connection to the MR head preamp, but you can interpose a cheap yet serviceable linear regulator fashioned from three transistors (**Figure 8**). This arrangement is adequate for most uses. Its output accuracy, however, depends on the VIN tolerance because (for simplicity) VIN serves as a reference for the regulator. The output ripple and noise are about 5mVp-p.

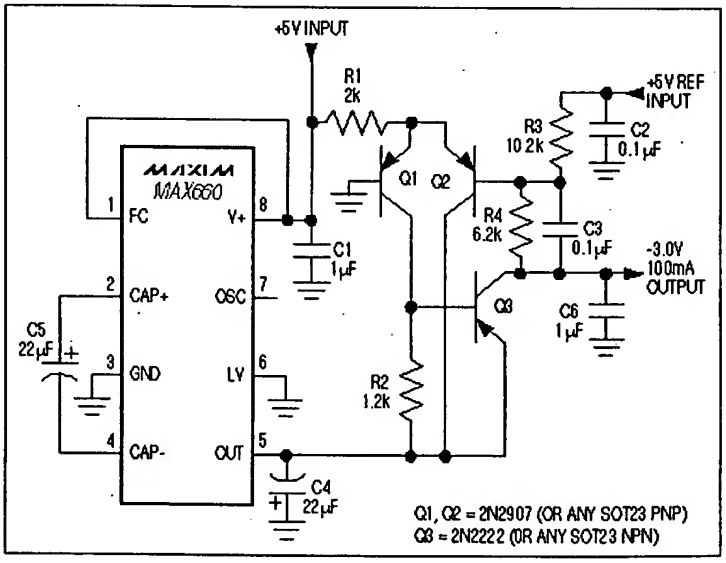


Figure 8. A cheap but serviceable three-transistor circuit adds a regulated 100mA, -3V output to a charge-pump IC.

Capacitor selection

A sometimes elusive bit of information relating to charge-pump designs is the minimum capacitor value needed for a particular load current. For most charge-pump ICs, the data sheet recommends only one or two capacitor values, yet (usually) the chip can operate with a wide range of values-especially when load currents are low. In most designs you should specify the smallest capacitor value that provides acceptable levels of output voltage, current, and ripple. These quantities depend on switching frequency and switch resistance as well as capacitance.

The effect of capacitance value on ripple and output current is illustrated by the eight graphs shown in **Figure 9** (and summarized in **Table 1**). Each graph includes five curves that supplement data-sheet information for three common charge-pump dc-dc converters from Maxim-the MAX660, MAX860, and MAX861:

1) MAX660, high-frequency mode (FC = V+), approximately 40kHz
2) MAX860, high-frequency mode (FC = OUT), approximately 100kHz
3) MAX860, medium-frequency mode (FC = GND), approximately 40kHz
4) MAX861, high-frequency mode (FC = OUT), approximately 200kHz
5) MAX861, medium-frequency mode (FC = GND), approximately 90kHz

These graphs show that lower load currents can often be supported by small ceramic capacitors. Evolving ceramic capacitor technology is producing higher values at lower costs, so you can now obtain ceramic capacitors to 10μF, at volume prices in the $0.30 range, from manufacturers such as United Chemicon (formerly Marcon), Tokin, TDK, and Murata Erie.

The frequency for each curve in Figure 9 is somewhat less than the typical found in the data sheet, because V_{IN} is specified on the low side: 4.5V = 5V - 10%, and 3.0V = 3.3V - 10%. Some of the graphs depict higher current at 2.0μF than at 2.2μF. That occurs because the 1μF and 2μF values are ceramic chips (with Z5U dielectric), and the values from 2.2μF up are tantalum types (AVX TPS series). Current and ripple data was collected by loading the outputs until V_{OUT} reached the value shown in Table 1. (Ripple improvement is negligible at higher values of capacitance.) V_{OUT} is higher at lower load currents, but -(V_{OUT}) never exceeds V_{IN}.

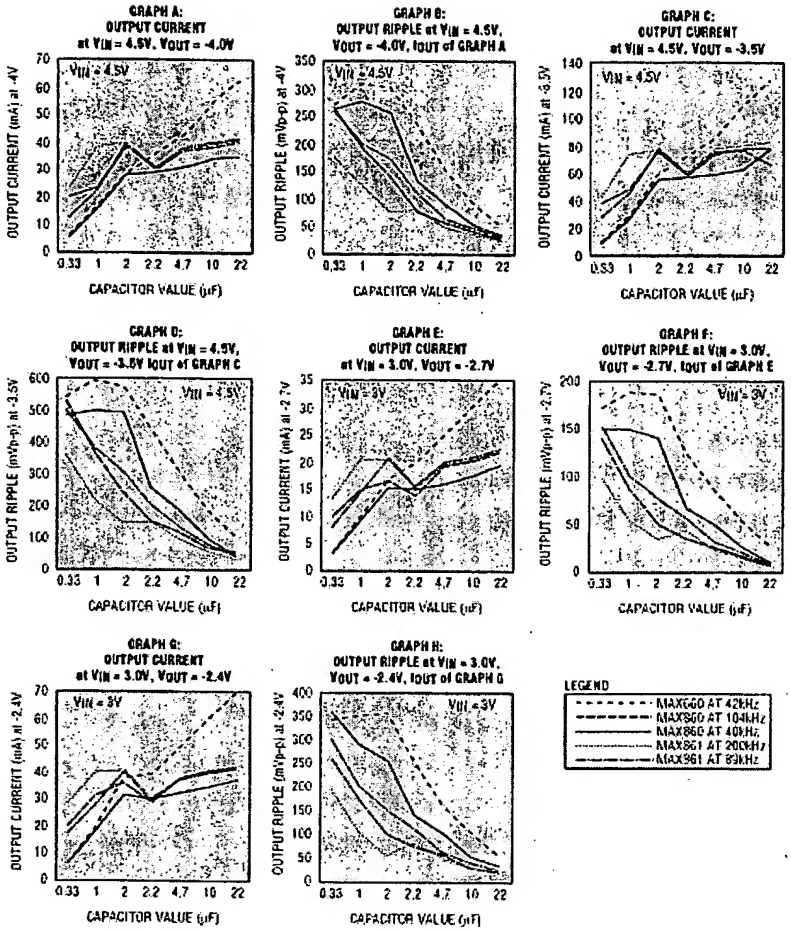


*Figure 9. These graphs (**A-H**) show the relationships among operating frequency, capacitance value, operating current, and output voltage for a charge-pump voltage converter. For a given load, the data enables selection of the minimum capacitance value and operating current.*

Table 1. Summary of graphs in Figure 9

GRAPH	V_{IN} (V)	V_{OUT} (V)	PLOTTED DATA
A	4.5	-4.0	I_{OUT} vs. cap. value (0.33µF to 22µF)
B	4.5	-4.0	Ripple vs. cap. value, at I_{OUT} from "A"
C	4.5	-3.5	I_{OUT} vs. cap. value
D	4.5	-3.5	Ripple vs. cap. value, at I_{OUT} from "C"

GRAPH	V_{IN} (V)	V_{OUT} (V)	PLOTTED DATA
E	3.0	-2.7	I_{OUT} vs. cap. value
F	3.0	-2.4	Ripple vs. cap. value, at I_{OUT} from "E"
G	3.0	-2.4	I_{OUT} vs. cap. value
H	3.0	-2.7	Ripple vs. cap. value, at I_{OUT} from "G"

Charge-pump tricks

Power conversion by integrated charge pumps is, of course, predated by the use of discrete capacitors for that purpose. Charge-pump techniques have been used in 50Hz/60Hz ac-line supplies for many years, and also in high-voltage multipliers to achieve outputs of several kV. The use of CMOS analog switches has enabled the integration of complex functions with very few parts. As another advantage, CMOS switches exhibit a virtual zero drop at low current, versus the

minimum 0.6V drop across a diode switch. But, in some cases, the addition of discrete components can add performance, even in applications employing the latest charge-pump ICs.

A low-power converter of 5V to ±20V can be made surprisingly small by enhancing a dual-output charge-pump IC with an extra boost stage composed of discrete diodes. Such supplies are useful for CCD power supplies, LCD bias, and varactor tuners. The MAX864 on its own can generate ±10V (minus load-proportional losses) from a 5V input, or ±6.6V from a 3.3V input. Using additional diode-capacitor stages (**Figure 10**), these outputs can be doubled again to approximately ±4VIN, or multiplied by 1.5 to approximately ±3VIN. Note that the external diode/capacitor network connects to C1 for ±15V outputs, or to C2 for ±20V outputs.

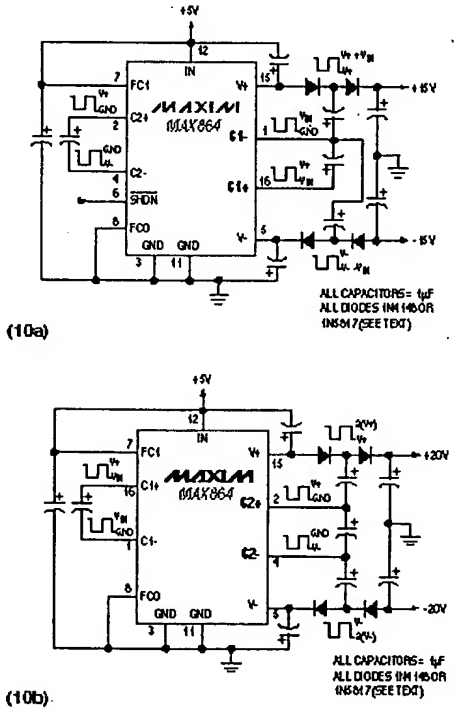


Figure 10. You can obtain higher output voltage from many charge-pump ICs by augmenting the circuit with external diodes and capacitors. These circuits supply up to ±20V.

Figure 11 illustrates the output voltage versus load current for each circuit in Figure 10, using both silicon diodes (for lowest cost) and Schottky diodes (for highest output). These circuits can supply as much as 20mA, and the 1µF filter capacitors yield less than 100mV of output ripple. If desired, you can lower that level considerably with slightly larger capacitors. The ICs in Figure 10 are set for 100kHz operation to allow use of 1µF capacitors, which results in a no-load supply current of 7mA. You can pin-program a lower frequency that lowers the supply current to 600µA, but to achieve the output currents shown in Figure 11 you'll need larger capacitors of 10µF.

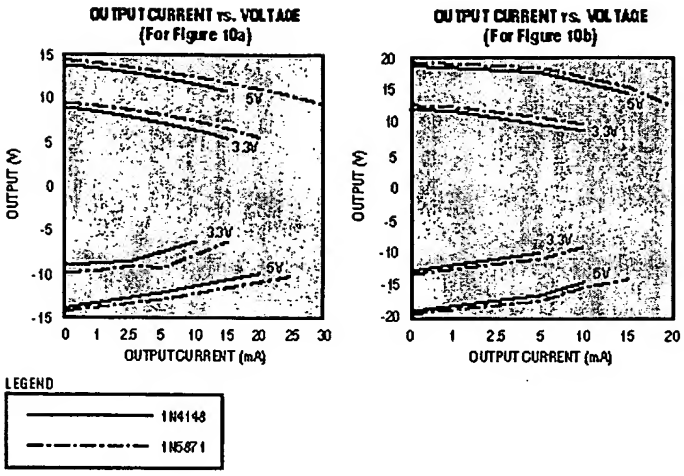


Figure 11. These graphs show VOUT vs. IOUT for the two circuits of Figure 10.

Normally, a single-stage charge-pump converter cannot generate negative outputs greater than its positive input voltage. To achieve negative outputs of -8V or more from inputs of 2.5V to 5.5V, add discrete diodes as shown in **Figure 12**. Peak-to-peak noise is the same as shown in Figure 7, and the available output current for a given regulated output voltage is shown at five discrete input voltages in **Figure 13**.

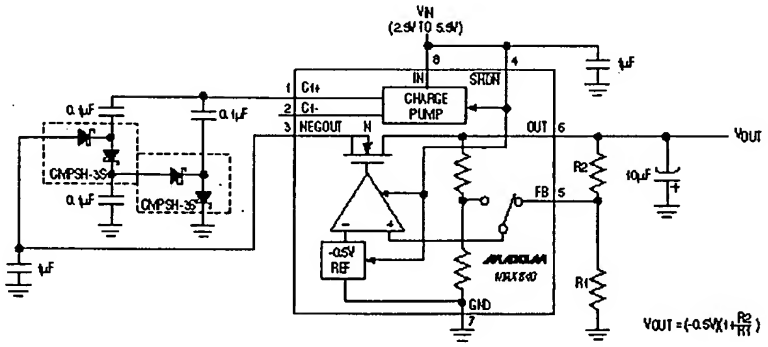


Figure 12. The diode-capacitor network external to this low-noise regulated charge pump lowers the minimum input voltage from 4.5V to 2.5V.

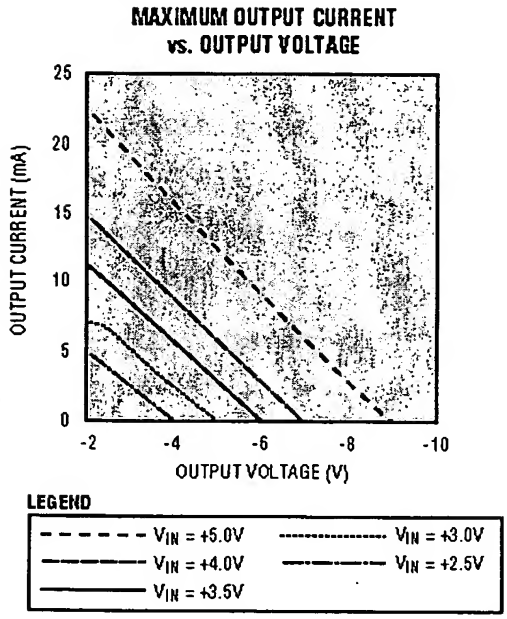


Figure 13. These curves show IOUT vs. regulated VOUT for the Figure 12 circuit.

To avoid the need to supply battery or line voltage to low-power computer peripherals, you can siphon off a few milliwatts from the serial port. The common PC mouse and other such designs rely on the modem control signals DTR and RTS, but the circuit of **Figure 14** gets power from the TX line of a 3-wire port. Its output capability (8mA) is sufficient for a CMOS microcontroller and some support electronics. The TX line idles at a negative voltage, so the IC's normal input polarity is reversed (the negative input voltage applied between the OUT pin and ground enables the IC to pump backward from its normal direction). Zener diode D1 provides shunt regulation for a 4.7V output.

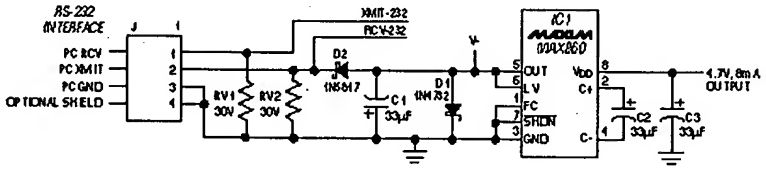


Figure 14. Operating in a voltage-doubler mode, this charge pump converts a negative input voltage (from the TX line of an RS-232 port) to a semi-regulated 5V output at 8mA.

Charge-pump ICs can help shrink the power supply in a portable system, so it pays to monitor the new technologies and new IC designs constantly being introduced by manufacturers. Maxim, for instance, offers a variety of charge-pump ICs, listed in **Tables 2-4**.

Table 2. Single-output charge pumps

PARAMETER	MAX828	MAX829	MAX860	MAX861	MAX660	MAX1044	ICL7662	ICL7660
PACKAGE	SOT23-5	SOT23-5	SO-8, µMAX	SO-8, µMAX	SO-8	SO-8	SO-8	SO-8, µMAX
OUTPUT CURRENT (mA typ)	0.06	0.15	0.2 @ 6kHz, 0.6 @ 50kHz, 1.4 @ 330kHz	0.3 @ 13kHz, 1.1 @ 100kHz, 2.5 @ 250kHz	0.12 @ 5kHz, 1 @ 40kHz	0.03	0.25	0.06
OUTPUT (Ω typ)	20	20	12	12	6.5	65	125	55
PUMP RATE (kHz)	12	35	6, 50, 130	13, 100, 150	5, 40	5	10	10
INPUT (V)	1.25 to 5.5	1.25 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 10	1.5 to 20	1.5 to 10

Table 3. Regulated charge pumps

PARAMETER	MAX619	MAX662A	MAX848/849/850	MAX850/1/2/3
PACKAGE	SO-8	SO-8	SO-8	SO-8
OUTPUT CURRENT (mA typ)	0.075	0.185	0.75	2
OUTPUT (V)	5±4%	12 ±5%	-2, or set -0.5 to -9.4	-4.1, or set -0.5 to -9
GUARANTEED IOUT (mA)	50	30	4	5
PUMP RATE (kHz)	500	500	100 ±20	100 ±20
INPUT (V)	2 to 3.6	4.5 to 5.5	2.5 to 10	4.5 to 10
SHUTDOWN	Yes	Yes	Yes	Yes
FEATURES/COMMENTS	—	Flash memory Vpp	Low-noise GaAsFET bias	Low-noise GaAsFET bias

Table 4. Multi-output charge pumps

PARAMETER	MAX680	MAX865	MAX864
PACKAGE	SO-8	µMAX	QSOP
OUTPUT CURRENT (mA typ)	1	0.6	0.6 @ 7kHz, 2.4 @ 33kHz, 7.0 @ 100kHz, 12 @ 195kHz
OUTPUT (V)	±10V (5V in)	±10V (5V in)	±10V (5V in)
POSITIVE Zout (Ω typ)	150	150	55
NEGATIVE Zout (Ω typ)	90	75	34
PUMP RATE (kHz)	8	24	7, 35, 100, 185
INPUT (V)	2 to 6	2 to 5	1.75 to 6
SHUTDOWN	No	No	Yes

features

- Regulated 3.3-V Output Voltage With up to 100-mA Output Current From a 1.8-V to 3.6-V Input Voltage
- Less Than 5-mV$_{(PP)}$ Output Voltage Ripple Achieved With Push-Pull Topology
- Integrated Low-Battery and Power-Good Detector
- Switching Frequency Can Be Synchronized to External Clock Signal
- Extends Battery Usage With up to 90% Efficiency and 35-μA Quiescent Supply Current
- Easy-to-Design, Low Cost, Low EMI Power Supply Since No Inductors Are Used
- 0.05-μA Shutdown Current, Battery is Isolated From Load in Shutdown Mode
- Compact Converter Solution in UltraSmall 10-pin MSOP With Only Four External Capacitors Required
- Evaluation Module Available (TPS60200EVM-145)

applications

- Replaces DC/DC Converters With Inductors in Battery Powered Applications Like:
  - Two Battery Cells to 3.3-V Conversion
  - MP3 Portable Audio Players
  - Battery-Powered Microprocessor Systems
  - Backup-Battery Boost Converters
  - PDA's, Organizers, and Cordless Phones
  - Handheld Instrumentation
  - Glucose Meters and Other Medical Instruments

description

The TPS6020x step-up, regulated charge pumps generate a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage. The devices are typically powered by two Alkaline, NiCd, or NiMH battery cells and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA from a 2-V input. Only four external capacitors are needed to build a complete low-ripple dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple, as current is continuously transferred to the output.

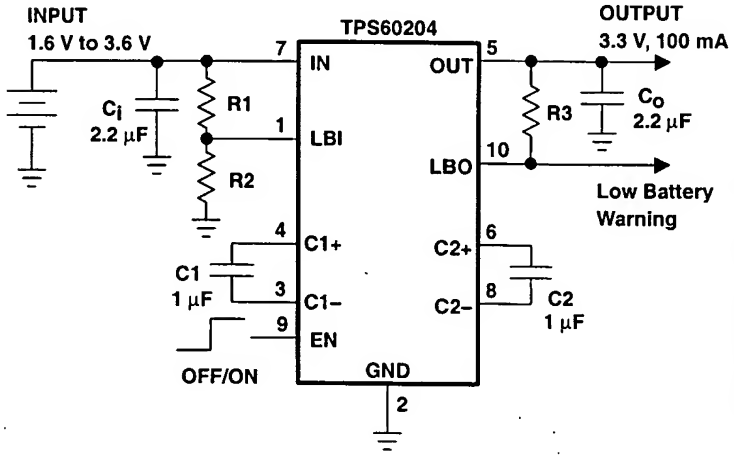
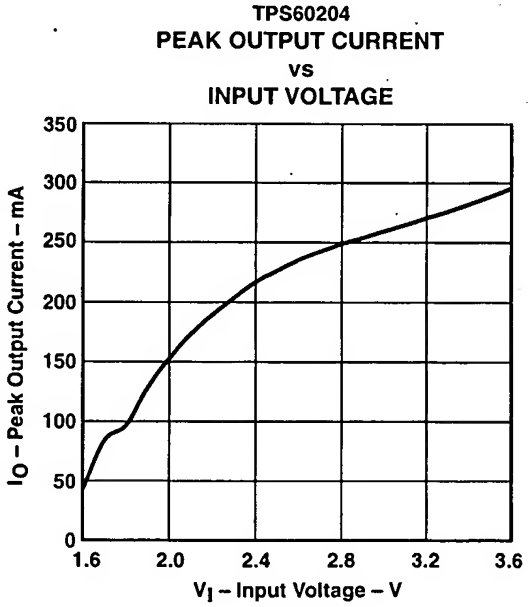


Figure 1. Typical Application Circuit With Low-Battery Warning



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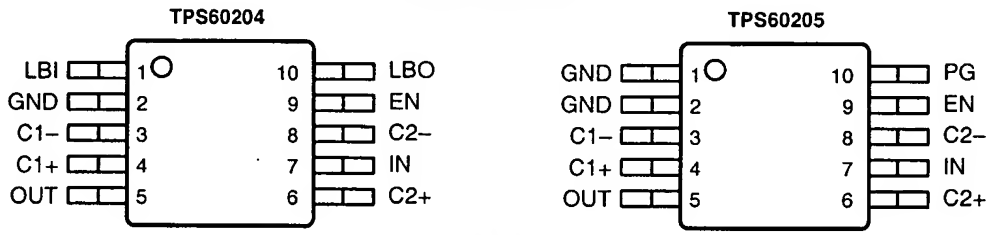
description (continued)

The devices operate in the newly developed LinSkip mode. In this operating mode, the device switches seamlessly from the power saving pulse-skip mode at light loads to the low-noise constant-frequency, linear-regulation mode once the output current exceeds the LinSkip threshold of about 7 mA. Even in pulse-skip mode, the output ripple is maintained at a very low level because the output resistance of the charge pump is still regulated.

Three operating modes can be programmed using the EN pin. EN = low disables the device, shuts down all internal circuits, and disconnects the output from the input. EN = high enables the device and programs it to run from the internal oscillator. The devices operate synchronized to an external clock signal if EN is clocked; thus, switching harmonics can be controlled and minimized. The devices include a low-battery detector that issues a warning if the battery voltage drops below a user-defined threshold voltage, or a power-good detector that goes active when the output voltage reaches about 90% of its nominal value.

Device options with either a low-battery or power good detector are available. This dc/dc converter requires no inductors, therefore, EMI of the system is reduced to a minimum. It is available in the small 10-pin MSOP package (DGS).

DGS PACKAGES



ACTUAL SIZE
3,05 mm x 4,98 mm

AVAILABLE OPTIONS

T_A	PART NUMBER†	MARKING DGS PACKAGE	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE (V)	DEVICE FEATURES
–40°C to 85°C	TPS60204DGS	AFB	100	3.3	Low-battery detector
	TPS60205DGS	AFC	100	3.3	Power-good detector

† The DGS package is available taped and reeled. Add R suffix to device type (e.g., TPS60204DGSR) to order quantities of 2500 devices per reel.

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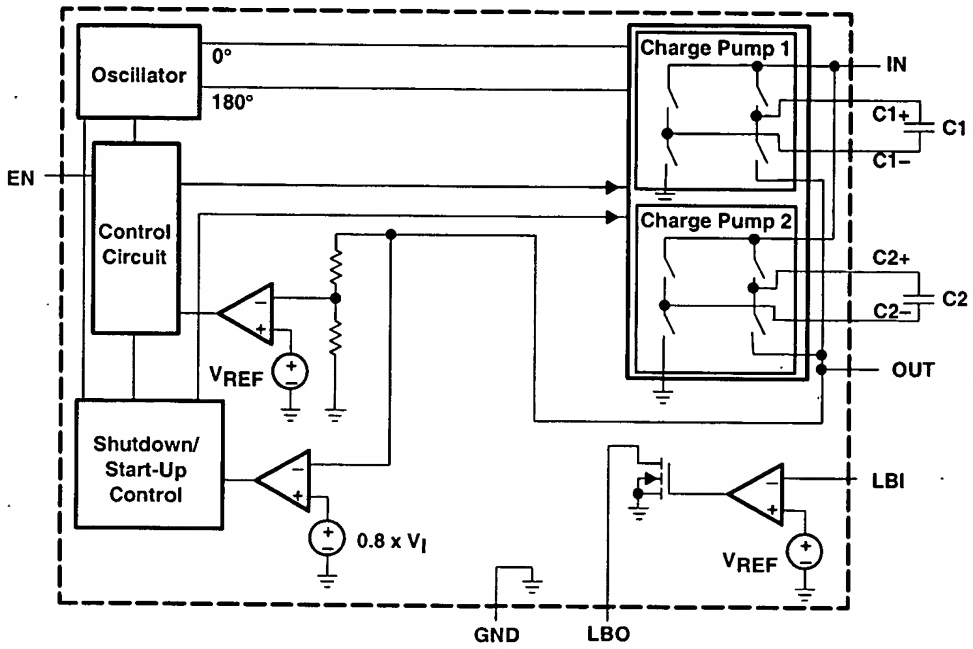
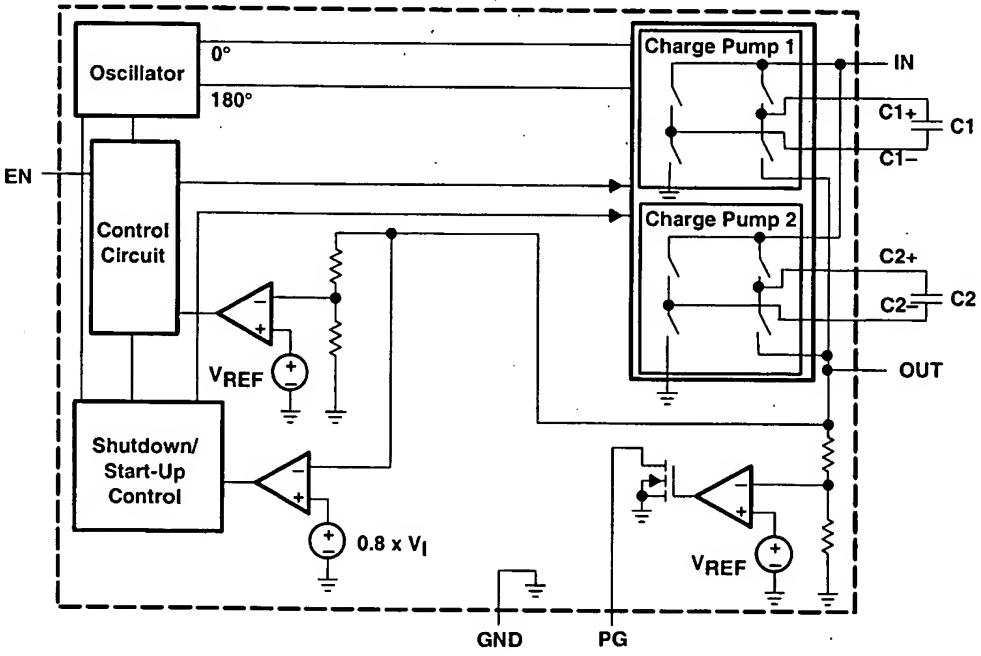
functional block diagrams

TPS60204 with low-battery detector



TPS60205 with power-good detector



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	4		Positive terminal of the flying capacitor C1
C1–	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2–	8		Negative terminal of the flying capacitor C2
EN	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. – EN = Low disables the device. Output and input are isolated in the shutdown. – EN = High lets the device run from the internal oscillator. – If an external clock signal is applied to the EN pin, the device is in syncmode and runs synchronized at the frequency of the external clock signal.
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_O.
LBI/GND	1	I	Low-battery detector input for the TPS60204. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the TPS60205, this pin has to be connected to ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for the TPS60204. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for the TPS60205. As soon as the voltage on OUT reaches about 90% of it is nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_O.

detailed description

operating principle

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V ±4%. Designed specifically for space critical battery powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (see functional block diagrams).

push-pull operating mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, i.e., they operate with a 180°C phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

detailed description (continued)

constant-frequency mode

When the output current is higher then the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the $r_{DS(ON)}$ of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

pulse-skip mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

start up and shutdown

During start-up, i.e. when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage V_O reaches $0.8 \times V_I$. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33-Ω or 66-Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 µA. The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the products shelf life.

synchronization to an external clock signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 µs.

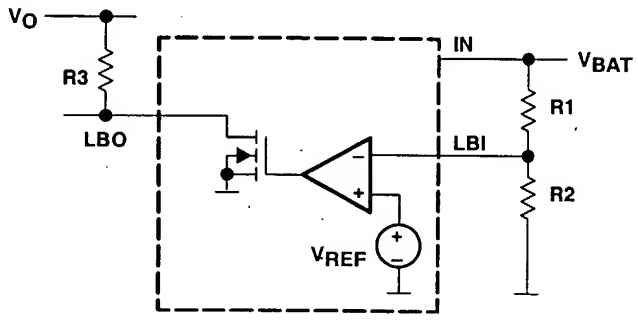
When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

detailed description (continued)

low-battery detector (TPS60204)

The low-battery comparator trips at 1.18 V ±4% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.



$$V_{(TRIP)} = 1.18\ V \left(1 + \frac{R1}{R2}\right)$$

Figure 2. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V_{LBI} = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\ M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

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detailed description (continued)

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

V_{IN}/V	R1/kΩ	R2/kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$/V
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

power-good detector (TPS60205)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range: IN, OUT, EN, LBI, LBO, PG to GND ..... –0.3 V to 3.6 V
C1+, C2+ to GND ..... –0.3 V to (V_O + 0.3 V)
C1–, C2– to GND ..... –0.3 V to (V_I + 0.3 V)
Continuous total power dissipation ..... See dissipation rating table
Continuous output current TPS60204, TPS60205 ..... 150 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	424 mW	3.4 mW/°C	187 mW	136 mW

The thermal resistance junction to ambient of the DGS package is R_{TH-JA} = 294°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	1.6		3.6	V
Input capacitor, C_i		2.2		µF
Flying capacitors, C1, C2		1		µF
Output capacitor, C_O		2.2		µF
Operating junction temperature, T_J	–40		125	°C

electrical characteristics at C_i = 2.2 µF, C1 = C2 = 1 µF, C_O = 2.2 µF, T_A = –40°C to 85°C, V_I = 2.4 V, EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	V_I = 2 V	100			mA
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17		3.43	
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	µA
$I_{(SD)}$	Shutdown supply current	EN = 0 V		0.05	1	
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	EN input high voltage	V_I = 1.6 V to 3.6 V	0.7 × V_I			
$I_{lkg(EN)}$	EN input leakage current	EN = 0 V or V_I		0.01	0.1	µA
	Output capacitor auto discharge time	EN is set from V_I to GND, Time until V_O < 0.5 V		0.6		ms
	Output leakage current in shutdown	EN = 0 V, T_A = –40 to 85°C			5	µA
		EN = 0 V, T_A ≤ 65°C			3	
	LinSkip threshold	V_I = 2.2 V		7		mA
	Output load regulation	10 mA < I_O < $I_{O(MAX)}$; T_A = 25°C		0.01		%/mA
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 x $I_{O(MAX)}$, T_A = 25°C		0.6		%/V
$I_{(SC)}$	Short circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

electrical characteristics for low-battery comparator of devices TPS60204 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6 V to 2.2 V, T_C = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		2	50	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	µA

NOTE: During start-up of the converter the LBO output signal is invalid for the first 500 µs.

electrical characteristics for power-good comparator of devices TPS60205 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_C = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_C = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage Low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	µA

NOTE: During start-up of the converter the PG output signal is invalid for the first 500 µs.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60204, TPS60205)	3
		vs Input voltage	4
I_Q	Quiescent supply current	vs Input voltage	5
V_O	Output voltage	vs Output current	6
		vs Input voltage	7
V_O	Output voltage ripple	vs Time	8, 9, 10
	Start-up timing		11
	Load transient response		12, 13
I_O	Peak output current	vs Input voltage	14

NOTE: All typical characteristics were measured using the typical application circuit of Figure 14 (unless otherwise noted).

TPS60204, TPS60205
EFFICIENCY
vs
OUTPUT CURRENT

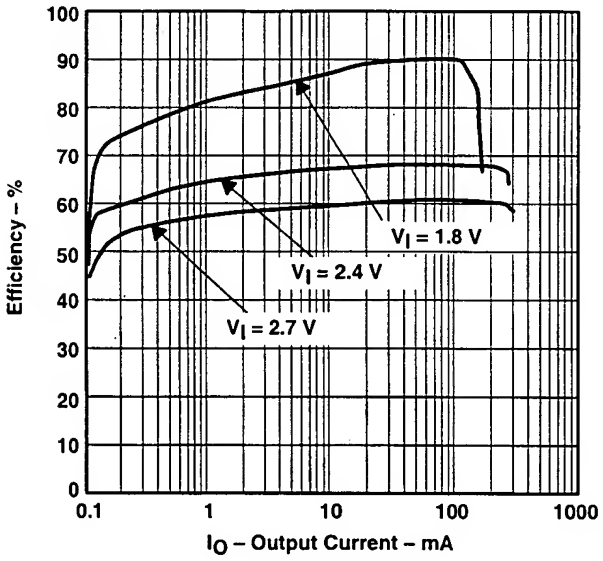

Figure 3

EFFICIENCY
vs
INPUT VOLTAGE

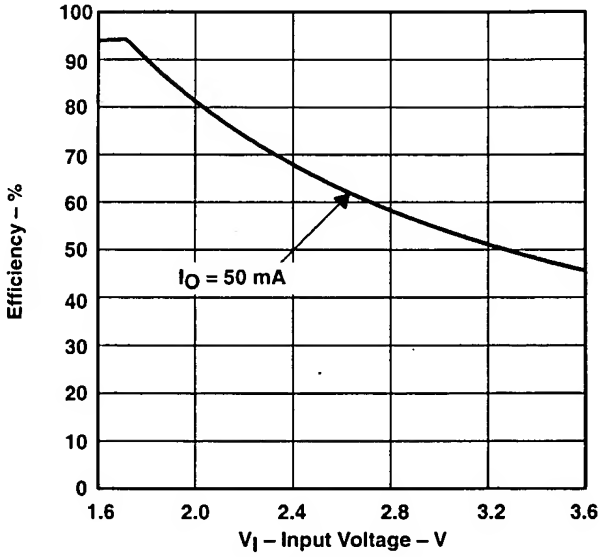

Figure 4

TYPICAL CHARACTERISTICS

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

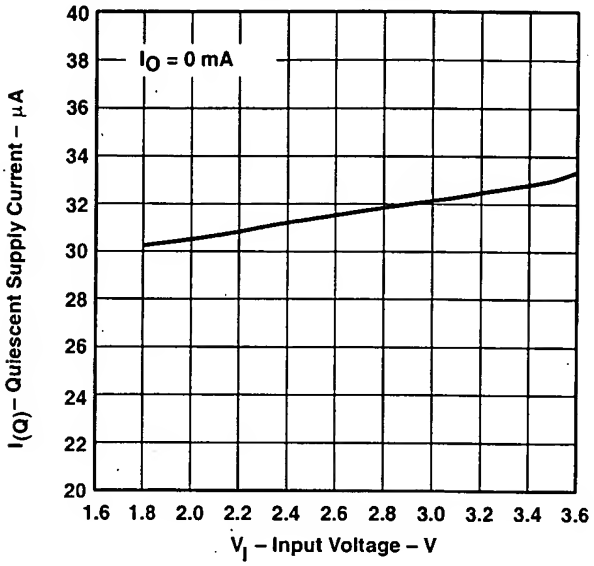

Figure 5

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

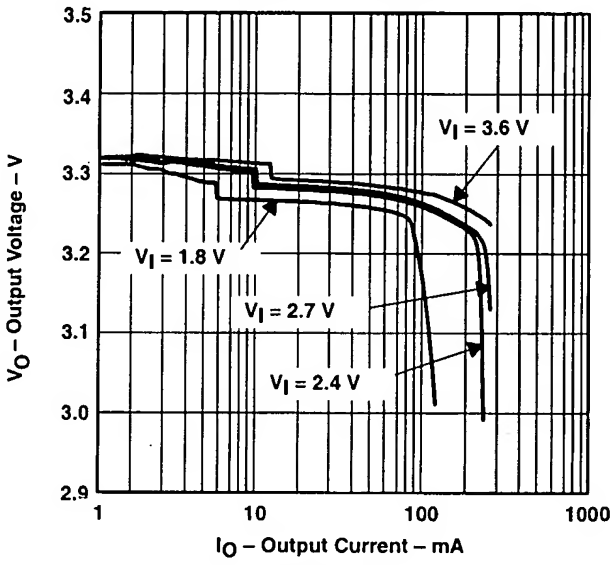

Figure 6

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

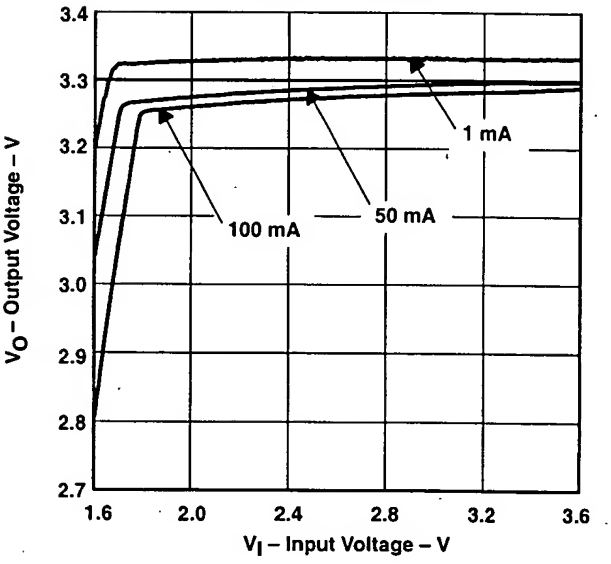

Figure 7

OUTPUT VOLTAGE RIPPLE
vs
TIME

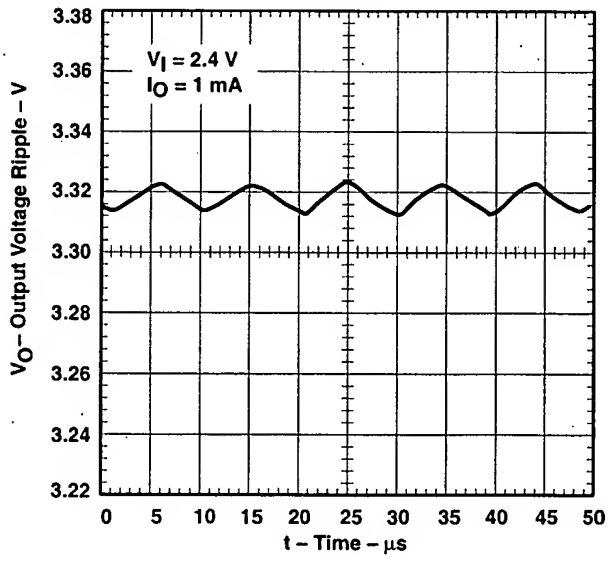

Figure 8

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RIPPLE
vs
TIME

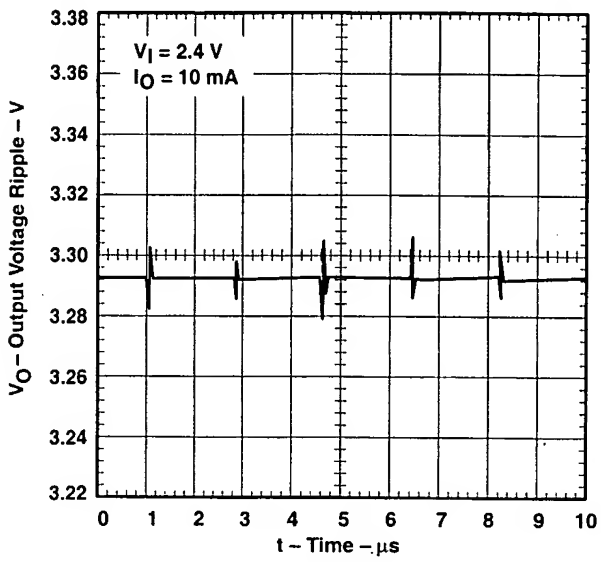

Figure 9

OUTPUT VOLTAGE RIPPLE
vs
TIME

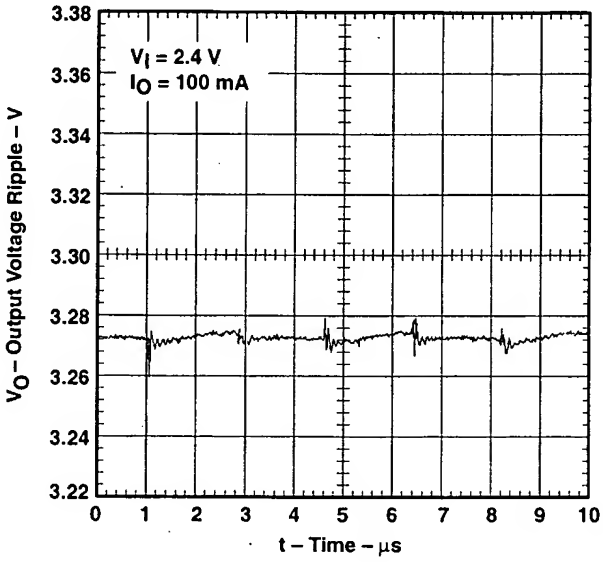

Figure 10

START-UP TIMING

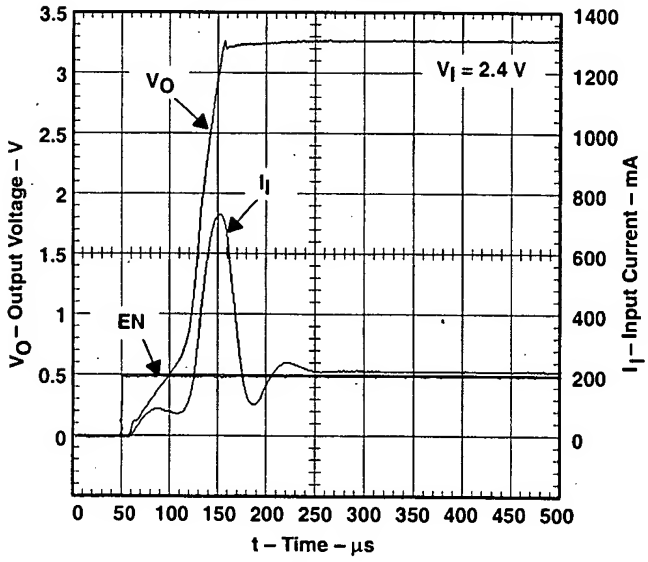

Figure 11

LOAD TRANSIENT RESPONSE

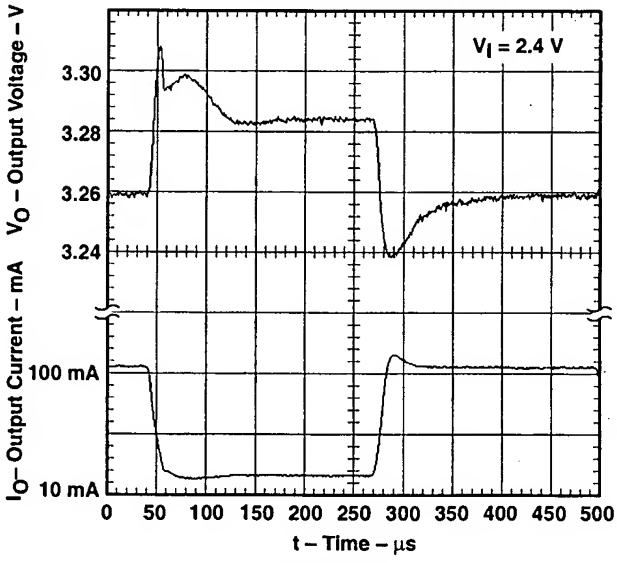

Figure 12

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

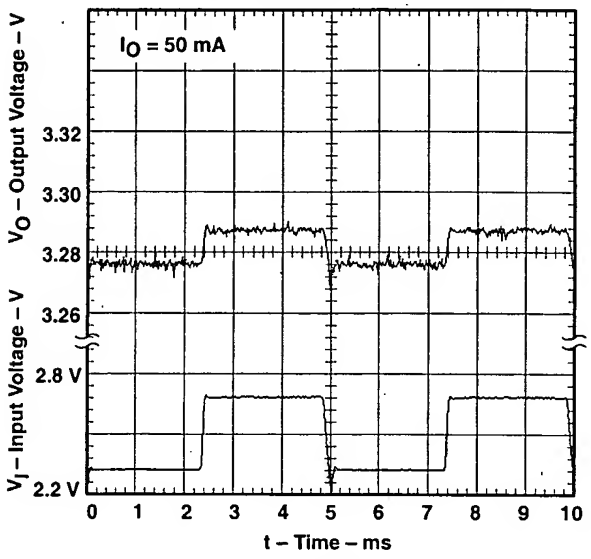

Figure 13

PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE

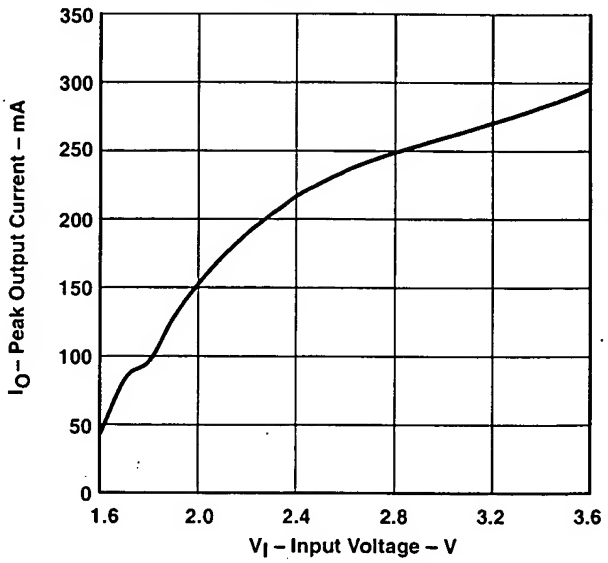

Figure 14

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APPLICATION INFORMATION

capacitor selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (<0.1 Ω) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest; a 1-µF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. C_i is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (C_o) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 µF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 2 lists the recommended capacitor values.

Table 2. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L (mA)	FLYING CAPACITORS, C1/C2 (µF)	INPUT CAPACITOR, C_i (µF)	OUTPUT CAPACITOR, C_o (µF)	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$ (mV)	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ (mV)
0–100	1	2.2	2.2	3	20
0–100	1	4.7	4.7	3	10
0–100	1	2.2	10	3	7
0–100	2.2	4.7	4.7	3	10
0–50	0.47	2.2	2.2	3	20
0–25	0.22	2.2	2.2	5	15
0–10	0.1	2.2	2.2	5	15

Table 3. Recommended Capacitor Types

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
	EMK212BJ224MG	0805	0.22 µF	Ceramic
	EMK212BJ474MG	0805	0.47 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106ML	1206	10 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

APPLICATION INFORMATION

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

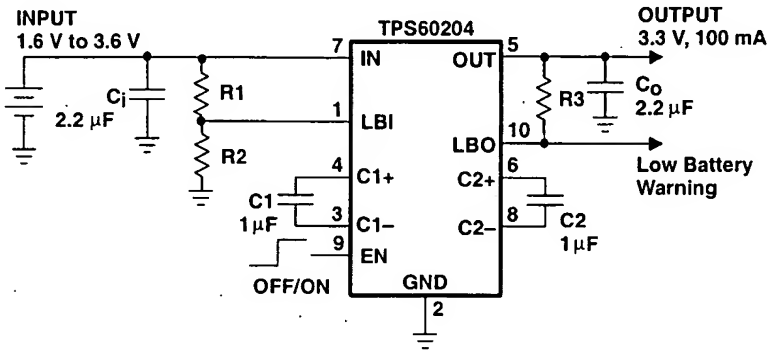


Figure 15. Typical Operating Circuit TPS60204 With Low-Battery Detector

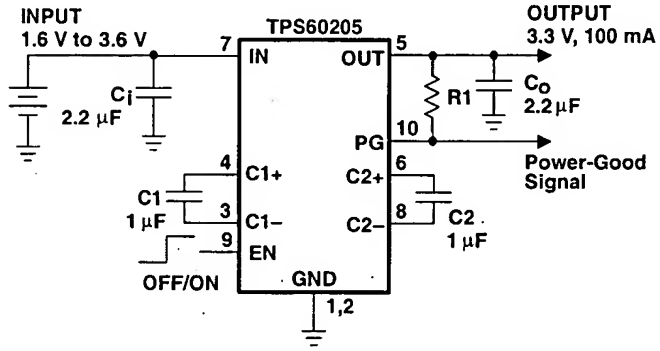


Figure 16. Typical Operating Circuit TPS60205 With Power-Good Detector

APPLICATION INFORMATION

power dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated by:

$$P_{(DISS)} = I_O \times \left(2 \times V_I - V_O\right) \quad \text{for } I_{(Q)} < I_O \tag{5}$$

By observing equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\Theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125°C - 85°C}{390\ mW} = 102°C/W \tag{6}$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\Theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However, in a battery powered application, both V_I and T_A will typically be lower than the worst case ratings used in equation 6 , and power dissipation should not be a problem in most applications.

layout and board space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 17. There is no specific EVM available for the TPS60204. However, the TPS60200EVM–145 can be used to evaluate the device.

The evaluation module for the TPS60200 can be ordered under product code TPS60200EVM–145. The EVM uses the layout shown in Figure 17. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket, therefore, the space needed for the IC, the external parts, and eight pins is 17,9 mm x 10,2 mm = 182,6 mm^2.

APPLICATION INFORMATION

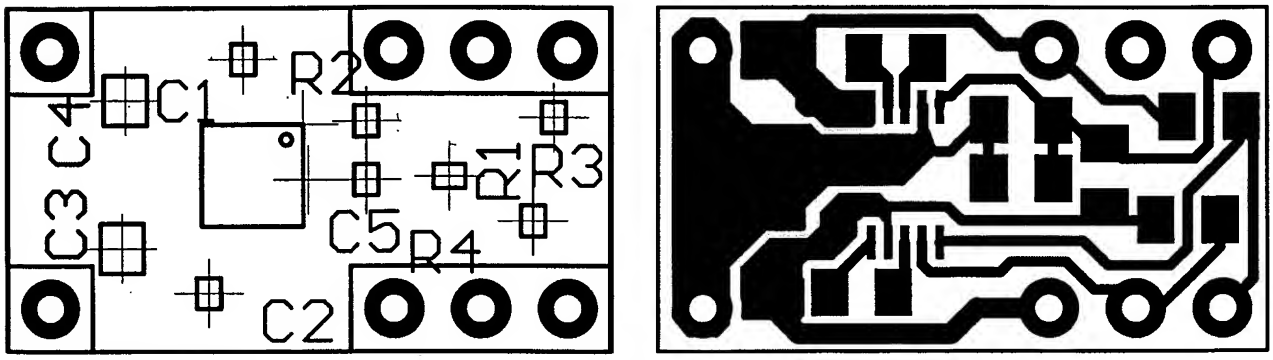


Figure 17. Recommended Component Placement and Board Layout

Table 5. Component Identification

IC1	TPS60204
C1, C2	Flying capacitors
C3	Input capacitors
C4	Output capacitors
C5	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

device family products

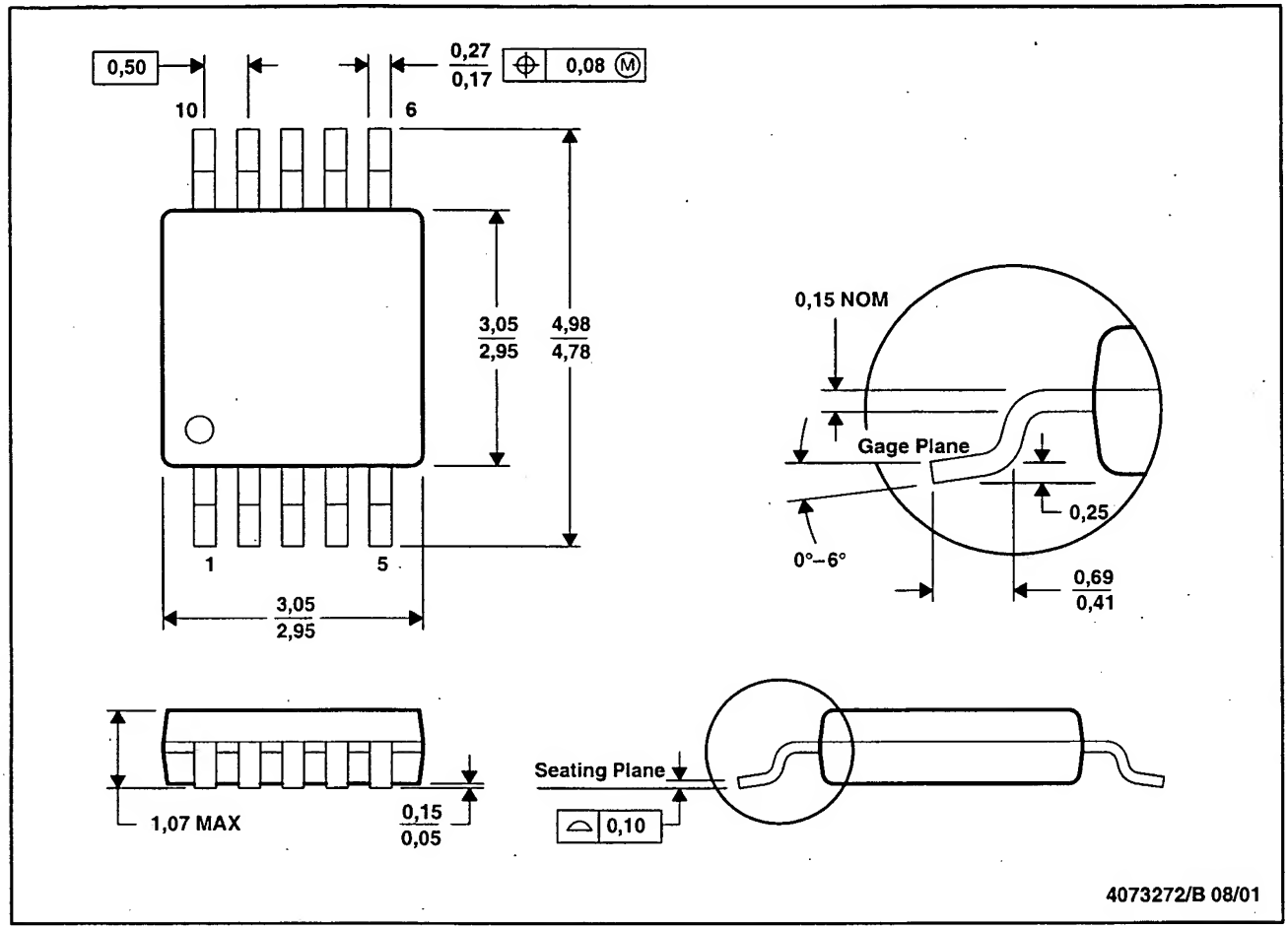
Other charge pump dc-dc converters in this family are:

Table 6. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5.0 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5.0 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with power-good comparator
TPS60132	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with power-good comparator

MECHANICAL DATA

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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LINEAR TECHNOLOGY

DESIGN NOTES

New Charge Pumps Offer Low Input and Output Noise

Design Note 243

Sam Nork

Charge pump (inductorless) DC/DC converters are quite popular in space-constrained applications where low to moderate load currents must be supplied. Such converters are available in small packages, operate with very low quiescent current and require minimal external components. However, noise generation is one undesirable characteristic of most charge pumps.

Unwanted noise can create a variety of problems. Noise generated at the power input can interfere with RF transmission and reception in wireless applicatons. Noise at the output can couple onto sensitive circuits or even create audible noise. The new LTC®3200 family of boost charge pumps employs a new architecture designed to minimize noise at the input and output to mitigate such unwanted behavior.

Burst Mode™ Operation vs Constant Frequency

Most regulating charge pump DC/DC converters operate using a Burst Mode architecture. Such regulator architectures provide the lowest quiescent current, but generate the highest levels of both input and output noise. With Burst Mode parts, the charge pump switches are either delivering maximum current to the output or are turned off completely. A hysteretic comparator and reference control the turn-on and -off of the charge pump to provide output regulation. Low frequency ripple appears at the output and is required for regulation (see Figure 1). This bursting on and off also results in large input ripple current that must be supplied by the input source. Any impedance in the input source creates voltage noise at the input. This noise must then be rejected by the rest of the circuitry powered from the same source.

The LTC3200 and LTC3200-5 have been designed to minimize both input and output noise. These parts are regulating boost charge pumps that can supply up to 100mA of output current. The LTC3200-5 produces a regulated 5V output and is available in a 6-lead SOT-23 package. The LTC3200 produces an adjustable output voltage and is available in an 8-lead MSOP package. Both parts use a constant-frequency architecture that eliminates low frequency output noise. Charge pump switching is continuous, even with no load, and a linear control loop regulates the amount of charge transferred to the output on each clock cycle. Since the output regulation loop is linear, the peak-to-peak output ripple can be approximated as $V_{RIPPLE} = (I_{LOAD}/C_{OUT})/(2 \bullet f_{OSC})$, with no additional ripple due to regulator hysteresis.

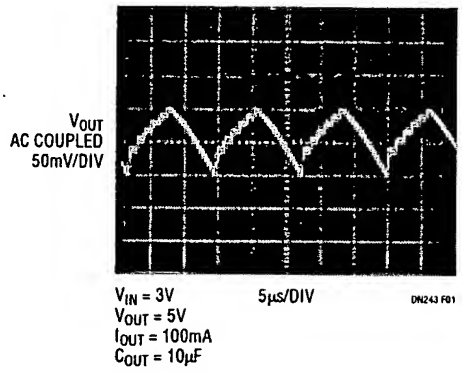

Figure 1. Typical Burst Mode Output Ripple

The parts' 2MHz oscillator frequency allows low output ripple to be achieved even with small output capacitors. Figure 2 illustrates the output ripple achievable with the LTC3200-5 supporting a 100mA load with different values of output capacitance.

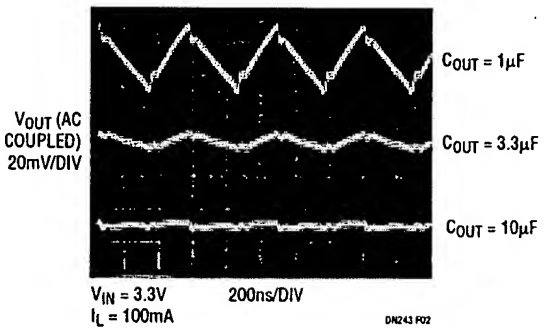

Figure 2. LTC3200-5 Output Ripple

Input Noise Reduction

Although constant frequency generation alone provides substantial input noise improvement, the LTC3200 family goes one step further. A unique internal control circuit regulates the input current on both phases of the charge pump clock. This technique prevents RC current decay during one or both half-clock cycles of the charge pump oscillator, thereby minimizing the input-referred ripple due to changing input current. Figure 3 shows the difference in input noise between the LTC3200 and a typical Burst Mode charge pump. Both parts are shown producing a regulated 5V output at 100mA of output current from a 3.6V input. 0.1Ω of input impedance is used for testing purposes. The typical Burst Mode part uses 10µF ceramic capacitors at both the input and the output. The LTC3200 uses 1µF ceramic caps of the same dielectric. As shown in Figure 3, significant improvements in input noise are achieved with the LTC3200—even with one-tenth the bypass capacitance.

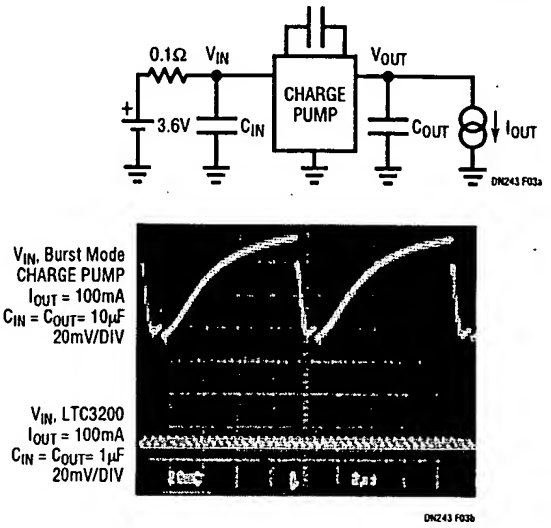

Figure 3. Input Noise Test Circuit

Typical Applications

Charge pumps are commonly used to provide low power boost conversion inside handheld devices such as cellular phones and PDAs. Such devices, particularly those which contain RF communication, tend to be very sensitive to noise. A popular application for a low noise charge pump in such products is powering white LEDs used for backlighting a small color LCD display. The circuit shown in Figure 4 produces a low noise boosted supply for driving up to six white LEDs. The LTC3200's FB pin is used to regulate the LED current flowing through each ballasted LED. By using the LTC3200, the user can provide boosted power to the backlight circuit directly from the battery without the cumbersome problem of filtering low frequency noise.

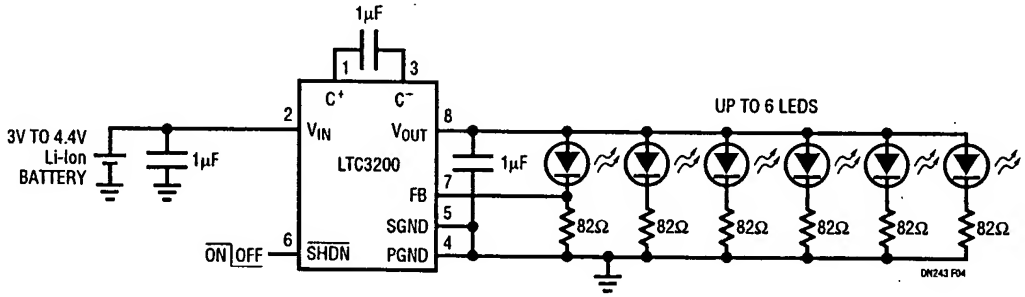

Figure 4. Low Noise White LED Driver with LED Current Control

Data Sheet Download

http://www.linear-tech.com/go/dnLTC3200

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Press Releases -- Dec 1998

LTC1550L/LTC1551L: Low Noise Charge Pump Inverters in MS8 Shrink Cell Phone Designs

MILPITAS, CA— December 4, 1998 — Linear Technology introduces the LTC1550L and LTC1551L, low-noise switched capacitor regulated voltage inverters for saving space in cell phones and similar applications. Designed for biasing GaAs FETs, both parts come in the compact 8-pin MSOP package and can operate from a single Li-Ion battery. Their 900kHz charge pump with a linear post regulator provides clean output with small components. This makes the LTC1550L and LTC1551L ideal for compact cell phone designs and in mobile radio and wireless modems and wireless LANs that need a well-regulated, low-noise negative bias supply. The LTC1550L and LTC1551L operate from a supply voltage (V_{CC}) of 2.7V to 5.5V and deliver an output voltage adjustable from -1.3V to -5.25V. Output current from a V_{CC} of 3.5V is 20mA at $-1.5V_{OUT}$ and up to 5mA at $-3.0V_{OUT}$. Output voltage regulation is ±2.5% and output ripple is less than $1mV_{P-P}$. Both parts also include a REG function to sense when output voltage is within 5% of a set value, which helps protect GaAs FETs that require a valid negative bias voltage at their gate before voltage is applied to the drain. The LTC1550L includes an active low Shutdown pin (SHDN) while the LTC1551L's Shutdown pin is active high. Both parts are available in fixed and adjustable output versions housed in 8-lead SO and MSOP packages; prices start at $1.70 per part per 1,000 pieces. The LTC1550L is also available in an adjustable 16-lead SSOP version priced at $1.90 per part per 1,000 pieces. All versions are available immediately from stock.

Summary of Features:

LTC1550L/LTC1551L Low Noise Charge Pumps

- Regulated negative voltage from a single positive supply
- Low output ripple: Less than 1mVP-P
- Output voltage regulation: ±2.5% over line, load and temperature
- Fixed -2V, -2.5V and –4.1V output or adjustable output (-1.5V to -4.5V)
- REG pin indicates when output voltage is within 5% of its regulated negative voltage
- Small charge pump capacitors (0.1μF)
- 900kHz charge pump frequency
- Requires only four external capacitors
- Shutdown mode drops supply current to <1μA
- High output current: Up to 20mA

Back to top

Accurate Phase Noise Prediction in PLL Synthesizers

Part 2: Here is a method that uses more complete modeling for wireless applications

By Lance Lascari
Adaptive Broadband Corporation

As discussed in part one of this article, published in the April issue of *Applied Microwave & Wireless*, phase noise characteristics of the frequency synthesizer contribute greatly to system performance. In this concluding section, we will show and discuss experimental results for the op-amp in loop filter.

Design goals	Value	Comments
Output Frequency	865 MHz	
Reference Frequency	200 kHz	
Frequency Step Size	12.5 kHz	
PLL Loop bandwidth	750 Hz	Get as close as possible with available components
Phase Margin	55 degrees	
Additional Reference Frequency Attenuation Required from the Third Pole	10 dB	

▲ **Table 2. Design goals for the example loop filter design.**

Op-amp in loop filter

While the cases using the passive loop filter (no op-amp) are simply a matter of circuit analysis, the case using the active filter requires some explanation. This case will only be described here; the accompanying analysis can be found in the supporting MathCad documents.

With the op-amp in the loop, and the filter configuration shown in Figure 1, four different noise sources and important factors exist within the loop itself: R_2, the op amp itself, the gain of the op-amp, and R_3.

The noise within R_2 is the same as the cases previously mentioned. However once this noise is determined, the gain of the amplifier needs to be applied to it (amp_gain in Figure 1). The output of the op-amp is again filtered by R_3 and C_3. A schematic of this is pictured in Figure 2a.

The op-amp itself contributes noise, and this is one reason to place the op-amp after the second order filter section but before the third pole. The third pole can then provide some attenuation of the broadband noise. Manufacturer's data sheets will usually specify the input noise of the op-amp in $nV/\sqrt{Hz}$. This noise voltage is simply multiplied by the amplifier's gain (amp_gain), and then passed through the filter formed by R_3 and C_3.

Op-amps are usually regarded as very low-output-impedance devices. For this reason, the analysis of the noise due to R_3 can be greatly simplified if an op-amp is in the loop as shown in Figure 1. If it is assumed that the op-amp output impedance is virtually a short (which would be accurate, even if the op-amp output were a few hundred ohms), then the noise voltage generated in R_3 is simply connected to ground, then filtered through R_3 and C_3.

Practical design example

To show the effect of the resistor noise, two different loop filters were designed to meet the basic specifications outlined in the goals section of Table 2. The only differences between the filters were their implementation of the third

pole. The values used in each of the designs were typical of what one designer might choose over another.

Experimental setup

Equipment used in the lab setup included a Hewlett-Packard 8563E spectrum analyzer with the phase noise utility software (P/N HP85671A) installed; a PC running a custom application developed to gather tabular data after the phase noise utility was run; and the PLL synthesizer under test (modified standard product produced by Adaptive Broadband Corporation).

The results presented in Figures 9 and 10 represent five averages of each phase noise measurement. In order to show the limitations of the measuring system, (i.e. the spectrum analyzer), the phase noise of the extremely low noise HP 8642B signal generator was plotted for comparison purposes. At higher offset frequencies where the measurements and models begin to disagree, it is clear that that the noise floor of the spectrum analyzer is contributing to measurement error.

Component/Specification	Value	Comments
Synthesizer IC, National LMX2350 Fractional-N PLL	Allows 1/16th Fractional mode	
Phase Detector Noise Floor (Npd_ref from Equation 6)	–200 dBc/Hz	Data supplied by National Semiconductor.
Phase Detector Gain	1.6 mA/cycle	Set to maximum for this design.
VCO Tuning Sensitivity, K_{vco}	27 MHz/volt	Custom vendor supplied component, measured at frequency of interest.
VCO Phase Noise	–103 dBc/Hz at 10 kHz offset	Measured for this particular device using a very narrow and quiet loop.
TCXO reference oscillator Frequency	12 MHz	
TCXO reference oscillator Phase Noise (Ntxco_ref from Equation 7)	–125 dBc/Hz at 100 Hz offset	This number was estimated from measurement data from many PLLs. This is roughly 10 dB worse than published data on a similar product from the TCXO vendor. Measurements for the model used were unavailable.

▲ **Table 3. Specifications for the components available.**

Discussion of experimental results

Figures 9 and 10 show excellent agreement between the modeled phase noise of the synthesizers and the measured results. The conclusion that must be drawn is resistor noise can be a very significant contributor to synthesizer phase noise, and thus needs to be considered in all low-noise synthesizer designs. For the case of these experiments, and others performed by the author, the models presented accurately predict this noise, allowing the analysis of all of these degradations at the time the loop is designed [1].

Loop Filter Component Values	Value for Case 1	Value for Case 2
C1	0.1 μF	0.1 μF
R2	500 ohms	500 ohms
C2	1 μF	1 μF
R3	1 kohm	10 kohm
C3	1000 pF	100 pF

▲ **Table 4. Component values for the two loop filters studied.**

The loop filters for case 1 and case 2 both meet the basic requirements of the design but have drastically different phase noise characteristics. For instance, at the 10 kHz offset points, the two synthesizers differ in phase noise by almost 10 dB. For narrowband systems with channels spaced at this interval, this would equate to a difference in adjacent channel rejection of 10 dB when comparing case 1 to case 2. Although the resistors are much smaller in the case 1 analysis, the noise contribution should not be ignored.

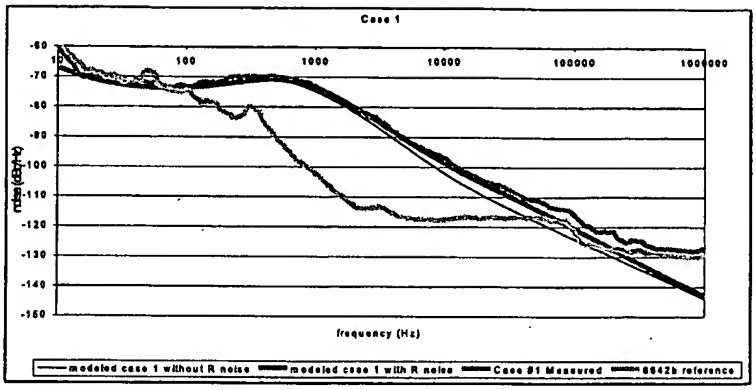
Even more significant than the agreement well outside of the loop bandwidth is the agreement near the loop bandwidth. Since the magnitude of the noise that falls near the loop corner is much larger than the noise far outside of the loop bandwidth, it contributes significantly to the RMS phase error and residual FM metrics. These metrics are very indicative of the performance degradations caused by frequency synthesizers in QAM and FM/FSK systems respectively. If the synthesizer noise were modeled without resistor noise, the results would be dramatically different, especially for case 2.

Reducing resistor and op-amp noise contributions

When designing a frequency synthesizer, there are

often several degrees of freedom that can be exercised in order to minimize the system phase noise. If there are no degrees of freedom, up-front design analysis will at least show an accurate prediction of the phase noise. This prediction may help to make system tradeoffs rather than sticking to a more stringent synthesizer specification.

In most synthesizer designs, it seems that R3 is typically the single most significant contributor to the resistor noise. This begs the question, "Is the third pole really needed?" If the reference suppression within the loop is sufficient without the third pole, it is in the designer's best interests to leave these parts out of the design. If this pole is required, the value of R_3 should be kept as small as possible without upsetting the basic filter response.



▲ **Figure 9. Measured and modeled phase noise of the example synthesizer, case 1.**

Some VCO designs themselves use resistors to supply the tuning voltage to the varactor (the similarity to the R_3 analysis is staggering). In many published VCO designs, large resistors are used to feed the varactor. This is a good choice for simple, and low-cost designs since resistors are inexpensive, resonance-free, and they don't typically degrade resonator Q if they're large relative to the other shunt resistances in the circuit. Resistors are hardly a good choice, however, if the tuning sensitivity (VCO gain) is high. The noise contribution by this resistor is proportional to its value alone in this case; a small resistor in series with a choke may be a good choice in many applications.

Op-amps, even if chosen carefully, represent significant contributions to phase noise. The synthesizer designer should be careful to determine whether an op-amp is truly required in order to meet the system requirements. If increased voltage is required, consider using an external charge pump with higher supply voltages (some synthesizer ICs still support the connections required for using an external charge pump). Obtaining good balance in an external charge pump can be difficult, leading to increased reference spurs and power supply noise at the reference frequency. A low noise charge pump potentially offers reduced noise over the op-amp, as the tuning voltage range can be increased with a designer-chosen charge pump current. This represents two degrees of freedom: lower tuning sensitivity and reduced resistor values due to potentially increased current. It would be excellent if the available synthesizer chips allowed for higher tuning voltages or specifically allowed for simple implementations of well-balanced external charge pumps.

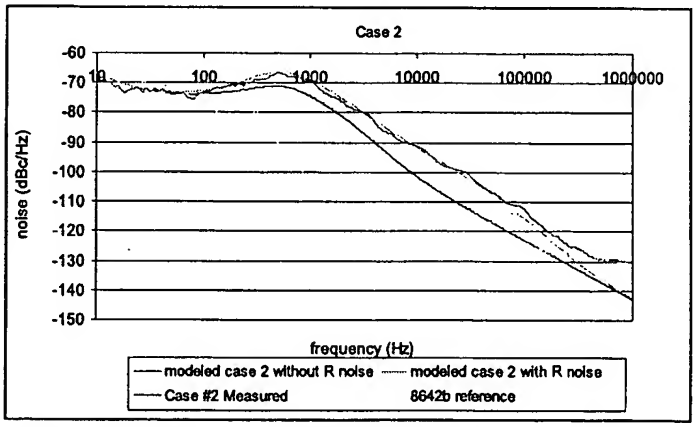
Reducing the VCO tuning sensitivity is another way to reduce the overall noise. This needs to be analyzed on a case-by-case basis, however, since the loop filter resistor values will increase with reduced tuning sensitivity. Any fixed magnitude noise sources in the loop will also drop proportionally with the VCO tuning sensitivity.

One particular option the author feels worthy of exploration is increasing charge pump current. With increased charge-pump current, the impedance (hence resistance) in the loop drops. If your synthesizer has a programmable charge pump current setting, leaving it at maximum is best in order to reduce the resistor noise contribution.

Each of the suggestions presented carries with it some design implication that needs to be carefully evaluated before tradeoffs are made. In some designs, simply increasing charge-pump current or eliminating the 3rd pole used for reference attenuation could yield dramatic improvement.

Conclusion

In order for designs to meet the increasingly demanding performance requirements in the wireless arena, a detailed understanding of every component is critical. While relatively simple, the models presented have demonstrated excellent accuracy when compared to experimental data. These circuit models represent new tools that enable the designer to make important tradeoffs during the initial synthesizer design phase, rather than on the bench using empirical and time-consuming techniques. ■



▲ **Figure 10. Measured and modeled phase noise of the example synthesizer, case 2.**

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